基本描述

LMX5050MK 高侧理想二极管控制器与外部 MOSFET 配合使用，当与电源串联时用作理想二极管整流器。该理想二极管控制器可使 MOSFET 替换主回路中的防反二极管，从而降低功耗和压降。

LMX5050MK 控制器为外部 N 沟道 MOSFET 和快速响应比较器提供电荷泵栅极驱动，在电流反向时关断 MOSFET。LMX5050MK 可连接 5V 至 100V 的电源，当输入电压在 1V 到 4V 之间时，VS 需要另外接 5V 以上的供电。

特性

♦ 宽工作输入电压范围 V_{IN}: 1V 到 100V （VIN < 5V 时需要 V_{BIAS}）

♦110V 瞬态电压

♦ 适用于外部 N 沟道 MOSFET 的电荷泵栅极驱动器

♦电流反向时可快速响应

♦2A 峰值栅极关断电流

♦超小 V_{DS} 关断电压，缩短关断时间

♦ SOT23-6L 封装

应用

冗余 (N+1) 电源的有源 OR-ing s

基本信息

器件信息

型号	描述
LMX5050MK	SOT23-6L
MPQ	3000pcs

封装耗散值

封装	RθJA（℃/W）
SOT-23 -6	108.1

极限值

参数	值
IN, OUT Pins to GND	-0.3 to 110V
GATE Pin to GND	-0.3 to 130V
VS Pin to Ground	-0.3 to 110V
OFF Pin to Ground	-0.3 to 7V
结温	150℃
存储温度，Tstg	-50 to 150℃
引脚焊接温度（soldering,10secs）	260℃
ESD 敏感性 HBM	±2000V

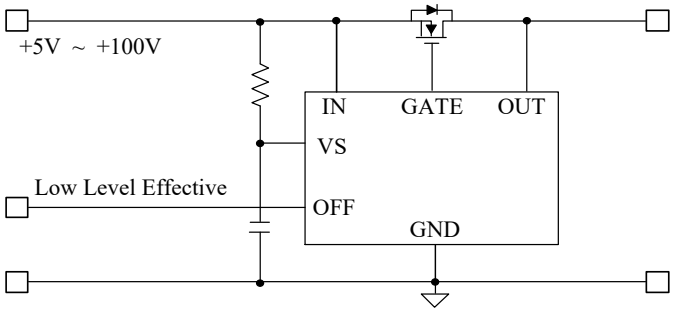
超出极限值中列出的范围可能会对设备造成永久性损坏。长时间工作在极限值条件下可能会影响可靠性。不建议设备在超出“推荐操作条件”部分中指示的任何条件下的功能运行。

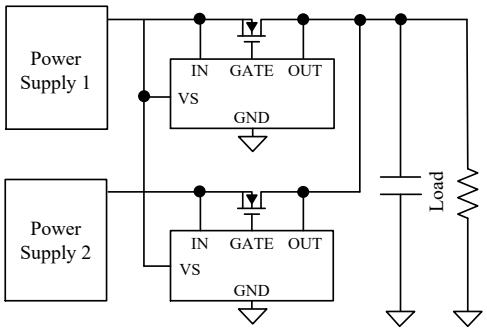
推荐工作条件

项目	范围
IN, OUT 引脚 （VS≥4.5V for IN＜4V）	1-100V
VS 引脚	5-100V
OFF 引脚	0-5.5V
工作温度	-40~125℃
湿度敏感等级	MSL3

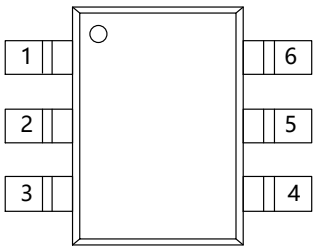
典型应用

VS is connected to VIN is recommended to reduce reverse leakage current during shutdown





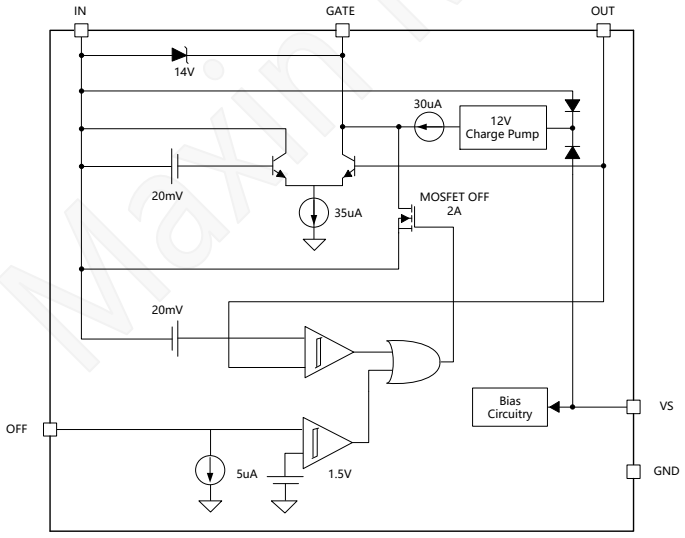
Terminal assignments



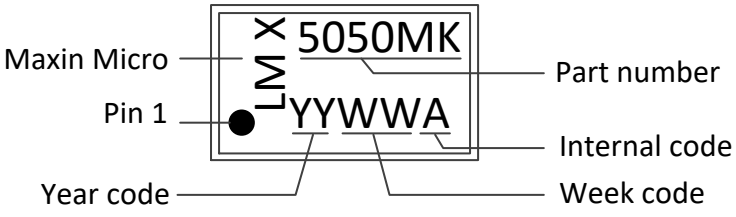
Pin information

PIN NO.	PIN name	Description
1	VS	The main supply pin for all internal biasing and an auxiliary supply for the internal gate drive charge pump. Typically connected to either V_{OUT} or V_{IN}. VS is connected to V_{IN} is recommended to reduce leakage current during reverse shutdown mode. A separate supply can also be used.
2	GND	Ground return for the controller
3	OFF	A logic high state at the OFF pin will pull the GATE pin low and turn off the external MOSFET. Note that when the MOSFET is off, current will still conduct through the FET's body diode. This pin should be left open or connected to GND if unused.
4	IN	Voltage sense connection to the external MOSFET Source pin.
5	GATE	Connect to the Gate of the external MOSFET. Controls the MOSFET to emulate a low forward-voltage diode.
6	OUT	Voltage sense connection to the external MOSFET Drain pin.

Block diagram



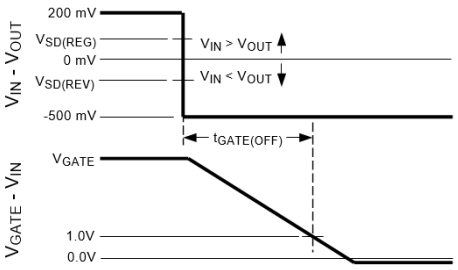
Marking information



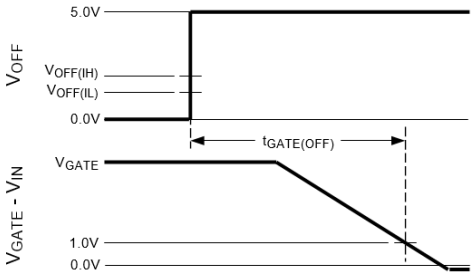
Electrical characteristics

（V_{IN} =12V, V_{VS} = V_{IN}, V_{OUT} = V_{IN}, V_{OFF} = 0V, C_{GATE} = 47nF, T_A = 25℃, unless otherwise noted）

Symbol	Parameter	Test condition	Min	Typ.	Max	Unit
VS PIN						
V_{VS}	Operating Supply Voltage Range		5		100	V
I_{VS}	Operating Supply Current	V_{VS} = 5V, V_{IN} = 5V, V_{OUT} = V_{IN} - 100mV		40	70	uA
		V_{VS} = 12V, V_{IN} = 5V, V_{OUT} = V_{IN} - 100mV		50	70	
		V_{VS} = 100V, V_{IN} = 5V, V_{OUT} = V_{IN} - 100mV		55	100	
IN PIN						
V_{IN}	Operating Input Voltage Range		1		110	V
I_{IN}	IN Pin current	V_{IN} =5V, V_{VS} = V_{IN}, V_{OUT} = V_{IN} -100mV, GATE = Open		350	400	uA
		V_{IN} = 12V to 100V, V_{VS} = V_{IN}, V_{OUT} = V_{IN} - 100mV, GATE = Open		500	600	
OUT PIN						
V_{OUT}	Operating Output Voltage Range		1		110	V
I_{OUT}	OUT Pin Current	V_{IN} = 5V to 100V, V_{VS} = V_{IN}, V_{OUT} = V_{IN} - 100mV		3.2	10	uA
GATE PIN						
$I_{GATE(ON)}$	Gate Pin Source Current	V_{IN} = 5V, V_{VS} = V_{IN}, V_{GATE} = V_{IN}, V_{OUT} = V_{IN} - 175mV	-33	-30	-23	uA
		V_{IN} = 12V to 100V, V_{VS} = V_{IN}, V_{GATE} = V_{IN} , V_{OUT} = V_{IN} - 175mV	-45	-35	-25	
V_{GS}	V_{GATE} – V_{IN} in Forward Operation	V_{IN} = 5V, V_{VS} = V_{IN}, V_{OUT} = V_{IN} - 175mV	6	8	10	V
		V_{IN} = 12V to 100V, V_{VS} = V_{IN}, V_{OUT} = V_{IN} - 175mV	8	12	14	
$t_{GATE(REV)}$	Gate Capacitance Discharge Time at Forward to Reverse Transition	C_{GATE} = 0		20		ns
		C_{GATE} = 10nF		120		
		C_{GATE} = 47nF		250		
$t_{GATE(OFF)}$	Gate Capacitance Discharge Time at OFF pin Low to High Transition	C_{GATE} = 47nF		1.2		us
$I_{GATE(OFF)}$	Gate Pin Sink Current	V_{GATE} = V_{IN} + 3V, V_{OUT} > V_{IN} + 100mV, t ≤ 10ms		2		A
$V_{SD(REV)}$	Reverse V_{SD} Threshold V_{IN} < V_{OUT}	V_{IN} - V_{OUT}	-30	-20	0	mV
$V_{SD(REG)}$	Regulated Forward V_{SD} Threshold V_{IN} > V_{OUT}	V_{IN} = 5V, V_{VS} = V_{IN}, V_{IN} - V_{OUT}	0	20	30	mV
		V_{IN} = 12V, V_{VS} = V_{IN}, V_{IN} - V_{OUT}	10	20	50	
OFF PIN						
$V_{OFF(IH)}$	OFF Input High Threshold Voltage	V_{OUT} = V_{IN} - 500mV, V_{OFF} Rising		1.57	1.8	V
$V_{OFF(IL)}$	OFF Input Low Threshold Voltage	V_{OUT} = V_{IN} - 500mV, V_{OFF} Falling	1.3	1.44		
ΔV_{OFF}	OFF Threshold Voltage Hysteresis	$V_{OFF(IH)}$ - $V_{OFF(IL)}$		155		mV
I_{OFF}	OFF Pin Internal Pulldown	V_{OFF} = 5V	2	5	8	uA



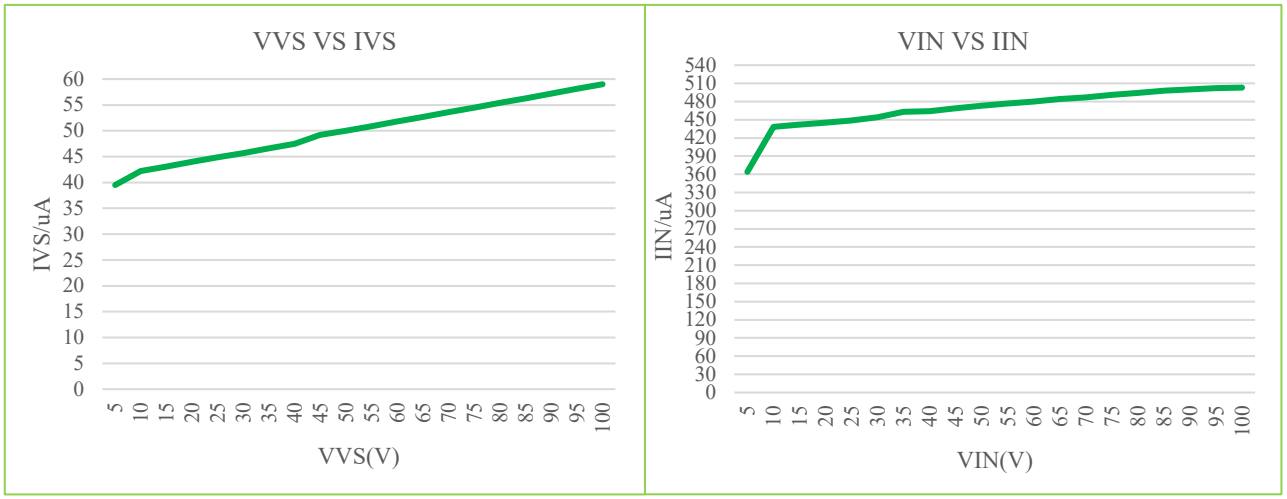
Gate OFF Timing for Forward to Reverse Transition

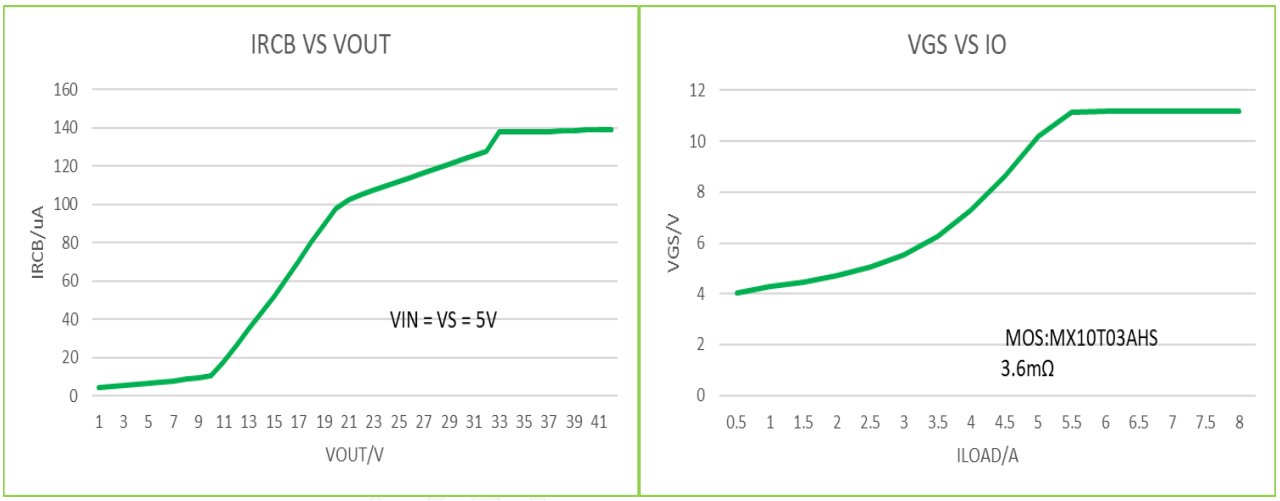


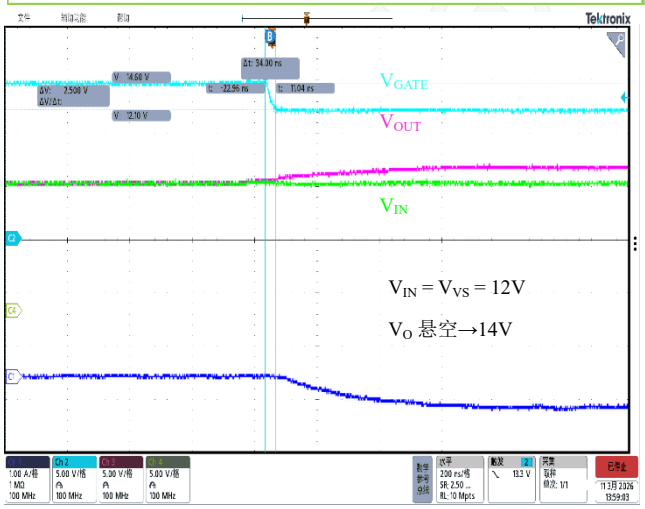
Gate OFF Timing for OFF Pin Low to High Transition

Characteristic plots

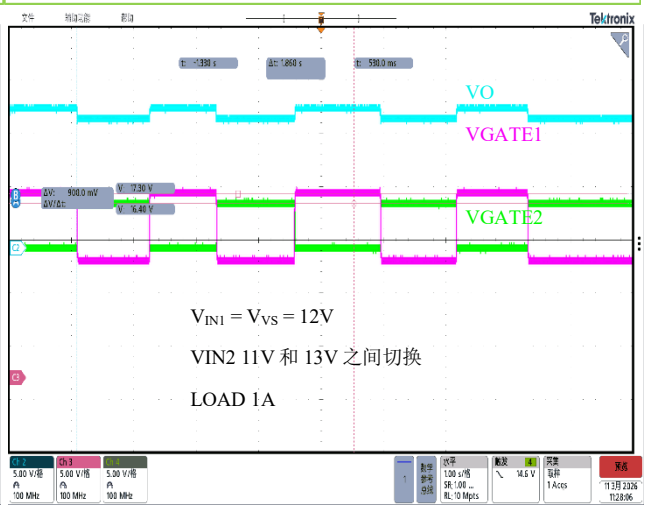
（V_{IN} = V_{VS} = V_{OUT}, V_{OFF} = 0V, T_A = 25℃, unless otherwise noted）



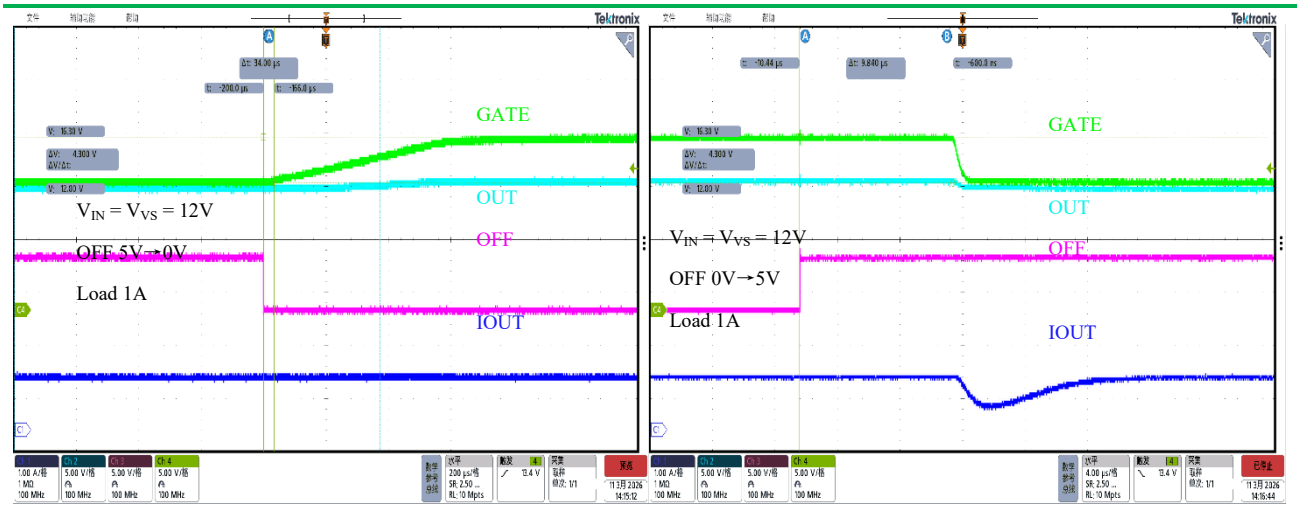




防倒灌波形



两路并联



OFF 启动波形 **OFF 关断波形**

Operation description

IN, GATE, and OUT Pins

When power is initially applied, the load current will flow from source to drain through the body diode of the MOSFET. Once the voltage across the body diode exceeds $V_{SD(REG)}$ then the LMX5050MK begins charging the MOSFET gate through a 30µA (typical) charge pump current source. In forward operation, the gate of the MOSFET is charged until it reaches the clamping voltage of the 14V GATE to IN pin Zener diode internal to the LMX5050MK.

The LMX5050MK is designed to regulate the MOSFET gate-to-source voltage. If the MOSFET current decreases to the point that the voltage across the MOSFET falls below the $V_{SD(REG)}$ voltage regulation point of 20mV (typical), the GATE pin voltage will be decreased until the voltage across the MOSFET is regulated at 20mV. If the source-to-drain voltage is greater than the $V_{SD(REG)}$ voltage, the gate-to-source voltage will increase and eventually reach the 14V GATE to IN pin Zener clamp level.

If the MOSFET current reverses, possibly due to failure of the input supply, such that the voltage across the LMX5050MK IN and OUT pins is more negative than the $V_{SD(REV)}$ voltage of -10mV (typical), the LMX5050MK will quickly discharge the MOSFET gate through a strong GATE to IN pin discharge transistor. If the input supply fails abruptly, as would occur if the supply was shorted directly to ground, a reverse current will temporarily flow through the MOSFET until the gate can be fully discharged. This reverse current is sourced from the load capacitance and from the parallel connected supplies. The LMX5050MK responds to a voltage reversal condition typically within 50ns. The actual time required to turn off the MOSFET will depend on the charge held by the gate capacitance of the MOSFET being used. A MOSFET with 47nF of effective gate capacitance can be turned off in typically 260ns. This fast turnoff time minimizes voltage disturbances at the output, as well as the current transients from the redundant supplies.

VS Pin

The VS pin of LMX5050MK is the main supply pin for all internal biasing and an auxiliary supply for the internal gate drive charge pump.

For typical LMX5050MK applications, the VS pin can be connected directly to the OUT pin. The capacitor value should be the lowest value that produces acceptable filtering of the voltage noise.

If VS is powered while IN is floating or grounded, then about 0.5mA will leak from the VS pin into the IC and about 2mA will leak from the OUT pin into the IC.

OFF Pin

The OFF pin is a logic level input pin that is used to control the gate drive to the external MOSFET. The maximum operating voltage on this pin is 5.5V.

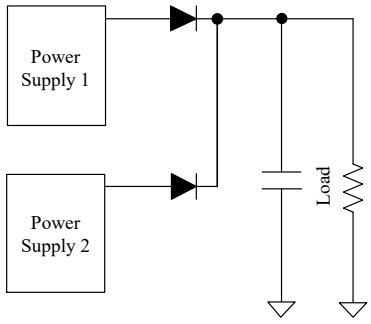
When the OFF pin is high, the MOSFET is turned off (independent of the sensed IN and OUT voltages). In this mode, load current will flow through the body diode of the MOSFET. The voltage difference between the IN pin and OUT pins will be approximately 700mV if the MOSFET is operating normally through the body diode.

The OFF pin has an internal pulldown of 5µA (typical). If the OFF function is not required, the pin may be left open or connected to ground.

Application and Implementation

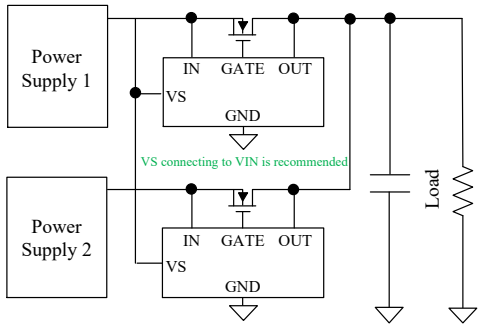
Application Information

Systems that require high availability often use multiple, parallel-connected redundant power supplies to improve reliability. Schottky OR-ing diodes are typically used to connect these redundant power supplies to a common point at the load. The disadvantage of using OR-ing diodes is the forward voltage drop, which reduces the available voltage and the associated power losses as load currents increase. Using an N-channel MOSFET to replace the OR-ing diode requires a small increase in the level of complexity, but reduces, or eliminates, the need for diode heat sinks or large thermal copper area in circuit board layouts for high power applications.



OR-ing with Diodes

The LMX5050MK is a positive voltage (that is, high-side) OR-ing controller that will drive an external N-channel MOSFET to replace an OR-ing diode. The voltage across the MOSFET source and drain pins is monitored by the LMX5050MK at the IN and OUT pins, while the GATE pin drives the MOSFET to control its operation based on the monitored source-drain voltage. The resulting behavior is that of an ideal rectifier with source and drain pins of the MOSFET acting as the anode and cathode pins of a diode respectively.



OR-ing With MOSFETs

MOSFET Selection

The important MOSFET electrical parameters are the maximum continuous Drain current I_D, the maximum Source current (that is, body diode) I_S, the maximum drain-to-source voltage $V_{DS(MAX)}$, the gate-to-source threshold voltage $V_{GS(TH)}$, the drain-to-source reverse breakdown voltage $V_{(BR)DSS}$, and the drain-to-source on resistance $R_{DS(ON)}$.

The maximum continuous drain current, I_D, rating must exceed the maximum continuous load current. The rating for the maximum current through the body diode, I_S, is typically rated the same as, or slightly higher than the drain current, but body diode current only flows while the MOSFET gate is being charged to $V_{GS(TH)}$.

Gate Charge Time = Qg / $I_{GATE(ON)}$

1. The maximum drain-to-source voltage, $V_{DS(MAX)}$, must be high enough to withstand the highest differential voltage seen in the application. This would include any anticipated fault conditions.

2. The drain-to-source reverse breakdown voltage, $V_{(BR)DSS}$, may provide some transient protection to the OUT pin in low voltage applications by allowing conduction back to the IN pin during positive transients at the OUT pin.

3. The gate-to-source threshold voltage, $V_{GS(TH)}$, should be compatible with the LMX5050MK gate drive capabilities. Logic level MOSFETs, with $R_{DS(ON)}$ rated at $V_{GS(TH)}$ at 5V, are recommended, but sub-Logic level MOSFETs having $R_{DS(ON)}$ rated at $V_{GS(TH)}$ at 2.5V, can also be used.

4. The dominate MOSFET loss for the LMX5050MK active OR-ing controller is conduction loss due to source-to-drain current to the output load, and the $R_{DS(ON)}$ of the MOSFET. This conduction loss could be reduced by using a MOSFET with the lowest possible $R_{DS(ON)}$. However, contrary to popular belief, arbitrarily selecting a MOSFET based solely on having low $R_{DS(ON)}$ may not always give desirable results for several reasons:

1. Reverse transition detection. Higher $R_{DS(ON)}$ will provide increased voltage information to the LMX5050MK Reverse Comparator at a lower reverse current level. This will give an earlier MOSFET turnoff condition should the input voltage become shorted to ground. This will minimize any disturbance of the redundant bus.

2. Reverse current leakage. In cases where multiple input supplies are closely matched it may be possible for some small current to flow continuously through the MOSFET drain to source (that is, reverse) without activating the LMX5050MK Reverse Comparator. Higher $R_{DS(ON)}$ will reduce this reverse current level.

3. Cost. Generally, as the $R_{DS(ON)}$ rating goes lower, the cost of the MOSFET goes higher.

5. The dominate MOSFET loss for the LMX5050MK active OR-ing controller is conduction loss due to source-to-drain current to the output load, and the $R_{DS(ON)}$ of the MOSFET. This conduction loss could be reduced by using a MOSFET with the lowest possible $R_{DS(ON)}$. However, contrary to popular belief, arbitrarily selecting a MOSFET based solely on having low $R_{DS(ON)}$ may not always give desirable results for several reasons:

a. Selecting a MOSFET with an $R_{DS(ON)}$ that is too large will result in excessive power dissipation. Additionally, the MOSFET gate will be charged to the full value that the LMX5050MK can provide as it attempts to drive the Drain to Source voltage down to the $V_{SD(REG)}$ of 20mV typical. This increased Gate charge will require some finite amount of additional discharge time when the MOSFET needs to be turned off.

b. As a guideline, it is suggested that $R_{DS(ON)}$ be selected to provide at least 20mV, and no more than 100mV, at the nominal load current.

c. $(20mV / I_D) \le R_{DS(ON)} \le (100mV / I_D)$

d. The thermal resistance of the MOSFET package should also be considered against the anticipated dissipation in the MOSFET to ensure that the junction temperature (T_J) is reasonably well controlled, because the $R_{DS(ON)}$ of the MOSFET increases as the junction temperature increases.

6. $P_{DISS} = I_D^2 \times (R_{DS(ON)})$

7. Operating with a maximum ambient temperature ($T_{A(MAX)}$) of 35°C, a current load of 10 A, and an $R_{DS(ON)}$ of 10 mΩ, and desiring to keep the junction temperature under 100°C, the maximum junction-to-ambient thermal resistance rating (θ_{JA}) must be:

a. $R_{\theta JA} \le (T_{J(MAX)} - T_{A(MAX)}) / (I_D^2 \times R_{DS(ON)})$

b. $R_{\theta JA} \le (100°C - 35°C) / (10A \times 10A \times 0.01\Omega)$

c. $R_{\theta JA} \le 65°C/W$

Short Circuit Failure of an Input Supply

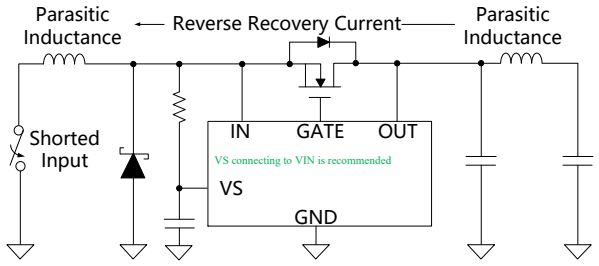
An abrupt 0Ω short circuit across the input supply will cause the highest possible reverse current to flow while the internal LMX5050MK control circuitry discharges the gate of the MOSFET. During this time, the reverse current is limited only by the $R_{DS(ON)}$ of the MOSFET, along with parasitic wiring resistances and inductances. Worst case instantaneous reverse current would be limited to:

$I_{D(REV)} = (V_{OUT} - V_{IN}) / R_{DS(ON)}$ (1)

The internal Reverse Comparator will react, and will start the process of discharging the Gate, when the reverse current reaches:

$I_{D(REV)} = V_{SD(REV)} / R_{DS(ON)}$ (2)

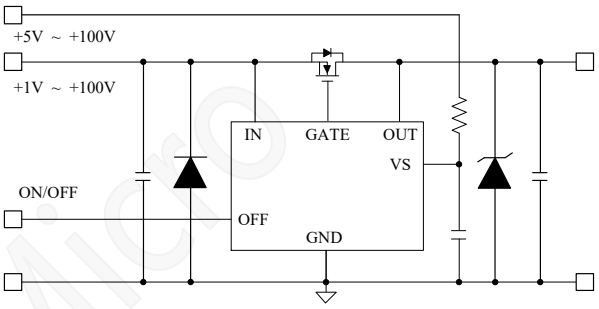
When the MOSFET is finally switched off, the energy stored in the parasitic wiring inductances will be transferred to the rest of the circuit. As a result, the LMX5050MK IN pin will see a negative voltage spike while the OUT pin will see a positive voltage spike. The IN pin can be protected by diode clamping the pin to GND in the negative direction. The OUT pin can be protected with a TVS protection diode, a local bypass capacitor, or both. In low voltage applications, the MOSFET drain to- source breakdown voltage rating may be adequate to protect the OUT pin (that is, $V_{IN} + V_{(BR)DSS(MAX)} <$ 100V), but most MOSFET data sheets do not ensure the maximum breakdown rating, so this method should be used with caution.



Reverse Recovery Current Generates Spikes at V_{IN} and V_{OUT}

A Separate VS Supply for Low Vin Operation

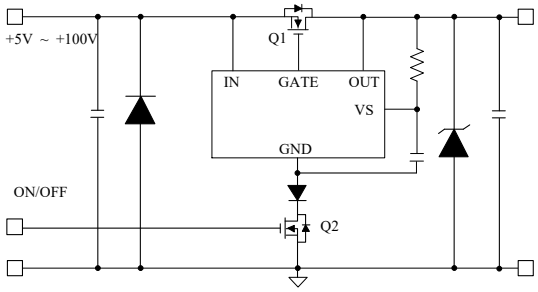
In some applications, it is desired to operate LMX5050MK from low supply voltage. The LMX5050MK can operate with a 1V rail voltage, provides its VS pin is biased from 5Vto 100V. The detail of such application is depicted in the next figure.



Reverse Input Voltage Protection with IQ Reduction

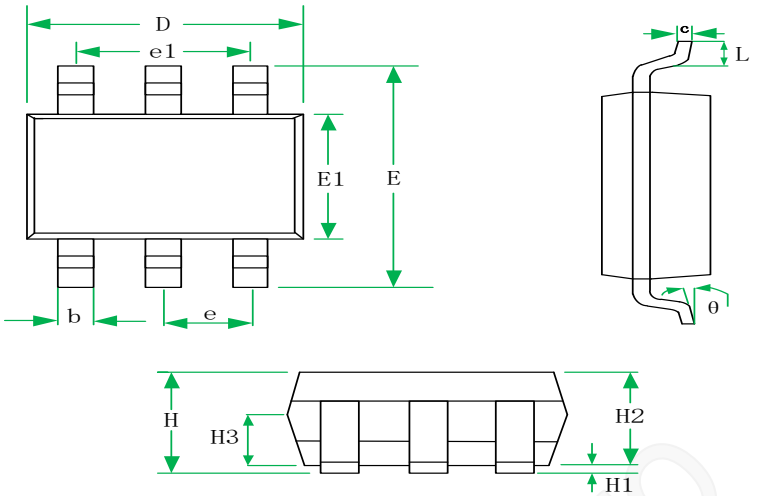
If VS is powered while IN is floating or grounded, then about 0.5mA will leak from the VS pin into the IC and about 3mA will leak from the OUT pin into the IC. From this leakage, about 0.05mA will flow out of the IN pin and the rest will flow to ground. This does not affect long-term reliability of the IC but may influence circuit design.

In battery powered applications, whenever LMX5050MK functionality is not needed, the supply to the LMX5050MK can be disconnected by turning OFF Q2, as shown in the following figure. This disconnects to the ground path of the LMX5050MK and eliminates the current leakage from the battery.



Reverse input voltage protection with IQ reduction schematic

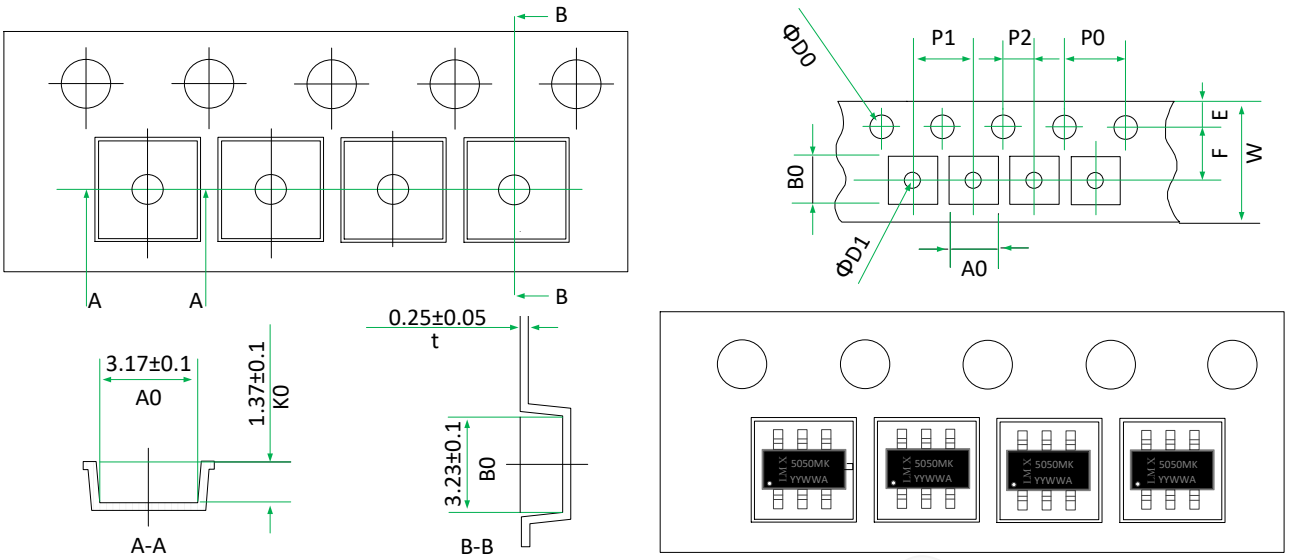
Package information



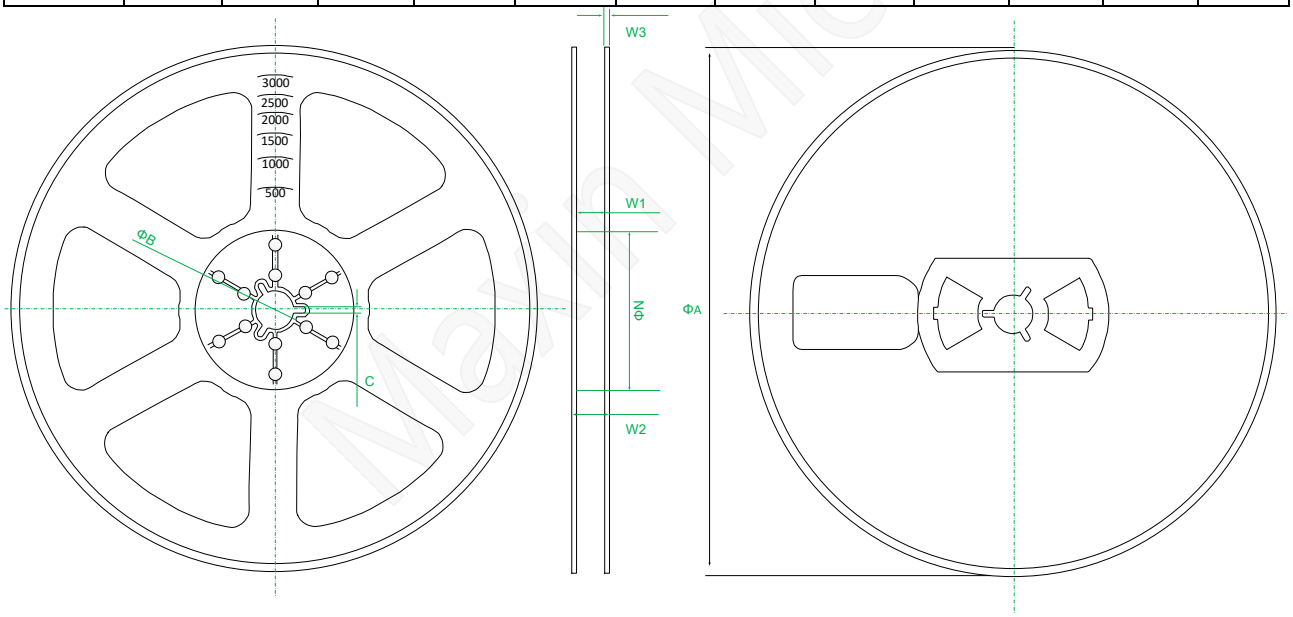
SYMBOL	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
H	1.07	1.16	1.25	0.042	0.046	0.049
H1	0.02	0.06	0.10	0.001	0.002	0.004
H2	1.05	1.10	1.15	0.041	0.043	0.045
H3	0.60	0.65	0.70	0.024	0.026	0.028
b	0.30	0.40	0.50	0.012	0.016	0.020
c	0.102	0.152	0.202	0.004	0.006	0.008
D	2.82	2.92	3.02	0.111	0.115	0.119
E	2.65	2.80	2.95	0.104	0.110	0.116
E1	1.50	1.60	1.70	0.059	0.063	0.067
e	0.95BSC			0.037BSC		
e1	1.90BSC			0.075BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
θ	0	4°REF	8°	0	4°REF	8°

SOT23-6 for LMX5050MK

Tape and Reel Information (unit in mm)



Symbol	W	E	F	ΦD0	ΦD1	P0	P1	P2	A0	B0	K0	t
MAX	8.10	1.85	3.55	1.60	1.25	4.10	4.10	2.05	3.27	3.33	1.47	0.30
MIN	7.90	1.65	3.45	1.40	1.0	3.90	3.90	1.95	3.07	3.13	1.27	0.20



Symbol	ΦA	ΦN	ΦB	C	W1	W2	W3
MAX	180	56	13.5	2.50	9.9	12	1.8
MIN	176	52	13.0	1.90	8.4		1.0

Restrictions on Product Use

◆ MAXIN micro is continually working to improve the quality and reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing MAXIN products, to comply with the standards of safety in making a safe design for the entire system, and to avoid situations in which a malfunction or failure of such MAXIN products could cause loss of human life, bodily injury or damage to property.

◆ In developing your designs, please ensure that MAXIN products are used within specified operating ranges as set forth in the most recent MAXIN products specifications.

◆ The information contained herein is subject to change without notice.

Version update record:

V10 The original version （preliminary）.