前言：

无锡明芯微电子于 2022 年发布了高边开关 MX5069D，MX5069MS 和 MX5069HD，这几款产品没有过流保护，功率限制和重启周期可调的功能，无锡明芯微在此基础上进行了技术迭代，发布了 LMX 系列产品，LMX5069 系列产品新增了功率限制，过流保护，软起动通过 Timer 可调等功能，并且在耐压和功耗上做了优化，工作和静态功耗都比国外同类产品减少一半，电压增加到 90V，最大耐压 108V。LMX5069 对之前发布的产品进行替代和升级，推荐客户用 LMX5069 做新产品设计。

1.特性

- 宽工作电压范围：9V 至 90V
- 浪涌电流限制，将电路板安全插入带电电源
- 可编程外部 MOS 的最大功耗
- 可调节电流限制
- 针对严重过流事件的断路器功能
- 适用于外部 N 沟道 MOSFET 的内部高侧电荷泵和栅极驱动器
- 可调节欠压锁定(UVLO)和迟滞
- 可调节过压锁定(OVLO)和迟滞
- 初始插入计时器可使振铃和瞬变在系统连接之后消除
- 可编程故障计时器可避免干扰性跳变
- PGOOD 开漏状态输出
- 10 引脚 MSOP 封装 和 10 引脚 DFN3x3-10L

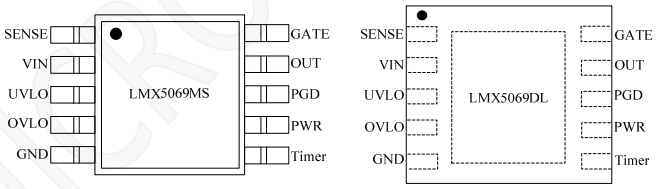
2 应用

- 服务器背板系统
- 基站配电系统
- 固态断路器
- 24V 和 48V 工业系统

3 说明

LMX5069 正电压热插拔控制器可在带电系统背板或其他热插拔电源插入和移除电路板期间为电源连接提供智能控制。LMX5069 可提供浪涌电流控制以限制系统电压的下降和瞬变。外部串行导通 N 沟道 MOSFET 中的电流限制和功率耗散可进行编程，从而确保 MOS 在安全工作区(SOA)内工作。当输出电压低于输入电压 1.5V 时，会显示电源正常输出。输入欠压和过压锁定电平和迟滞，以及初始插入延迟时间和故障监测时间均可进行编程。在故障监测时 LMX5069 以固定占空比自动重启。

4.引脚示意



General description

The LMX5069 high-side N_FET driver works with an external MOSFET and acts as hot swap controller with power limiting function. The LMX5069 is designed to control the in-rush current to the load upon insertion of a circuit card into a live backplane or other hot power source, thereby limiting the voltage sag on the backplane's supply voltage and the dV/dT of the voltage applied to the load.

The current limit in the external series pass N-Channel MOSFET is programmable. The input undervoltage and overvoltage lockout levels are programmable by resistance divider networks. The LMX5069 automatically restarts at a fixed duty cycle programmed by the Timer capacitor.

LMX5069 is available in 10-pin DFN3*3 and MSOP package.

Features

♦ Wide operating range: 9V to 90V

♦ Adjustable current limit

♦ Circuit breaker function for severe overcurrent events

♦ Internal high side charge pump and gate driver for external N-channel MOSFET

♦ Adjustable undervoltage lockout (UVLO)

♦ Adjustable overvoltage lockout (OVP)

♦Open drain POWER GOOD output

♦ Available with automatic restart

♦ 10-Pin DFN3*3-10L and MSOP10 package

Applications

♦ Server backplane systems

♦ Base station power distribution systems

♦ 24V and 48V Industrial systems

♦ Programmable logic circuit

♦ Solid state circuit breaker

General information

Ordering information

Part Number	Description
LMX5069DL	DFN3*3-10L
LMX5069MS	MSOP10
MPQ	3000pcs

Package dissipation rating

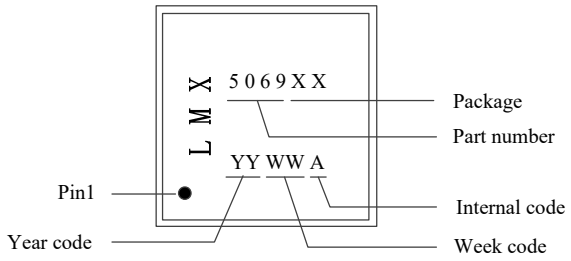
Package	RθJA（℃/W）
DFN3*3-10L	50
MSOP10	156

Absolute maximum ratings

Parameter	Value
VIN to GND	-0.3 to 108V
SENSE, OUT to GND	-0.3 to 108V
GATE to GND	-0.3 to 120V
OUT to GND (1ms transient)	-0.3 to 108V
OVP, PWR, Timer to GND	-0.3 to 7V
VIN to SENSE	-0.3 to 0.3V
Maximum junction temperature, T_{JMAX}	150℃
Storage temperature, T_{stg}	-65 to 150℃

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

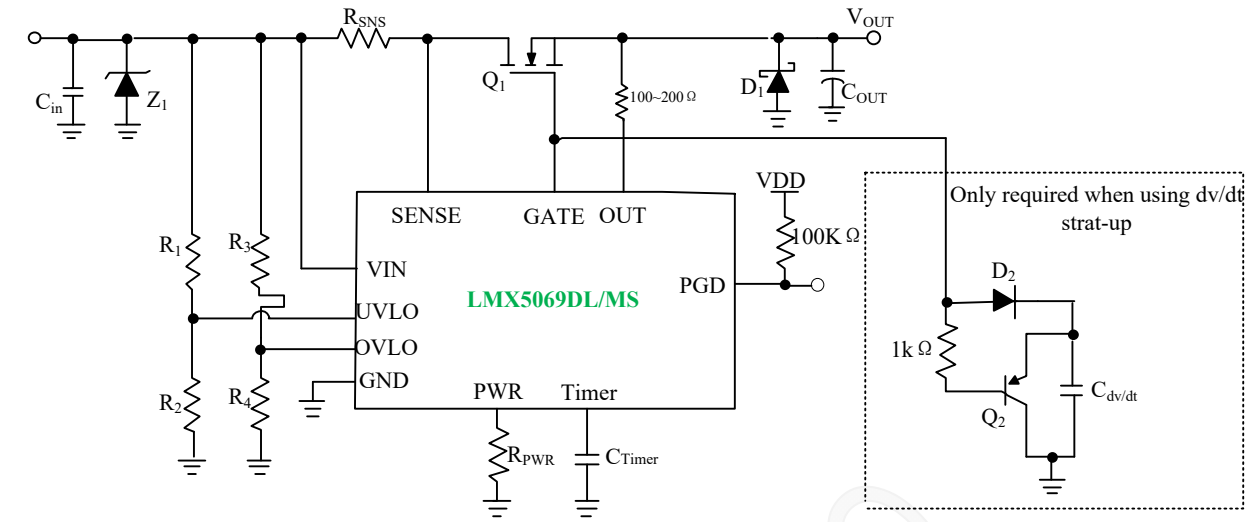
Marking information

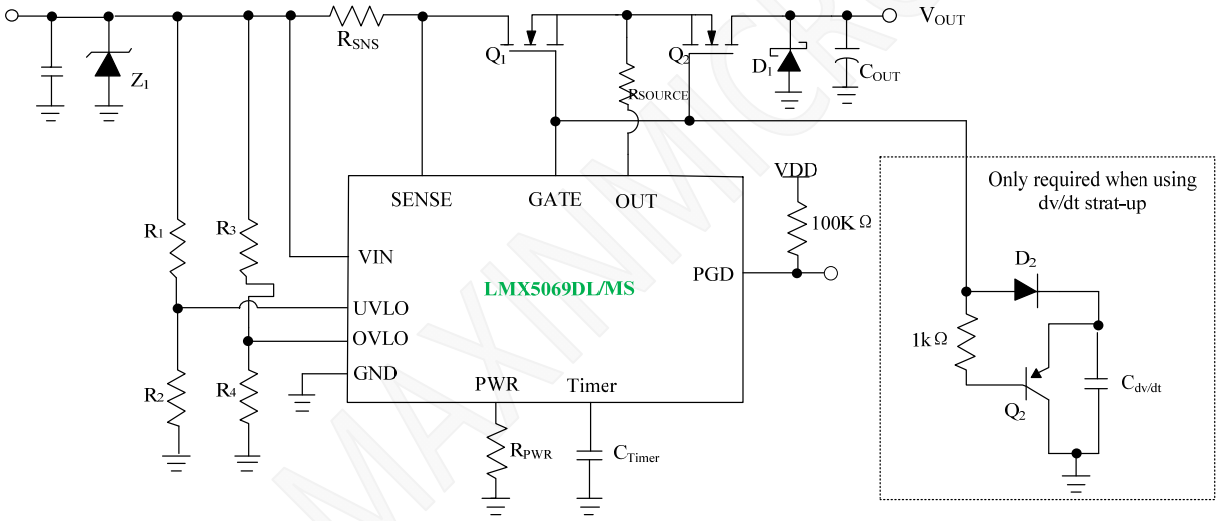


Recommended operating condition

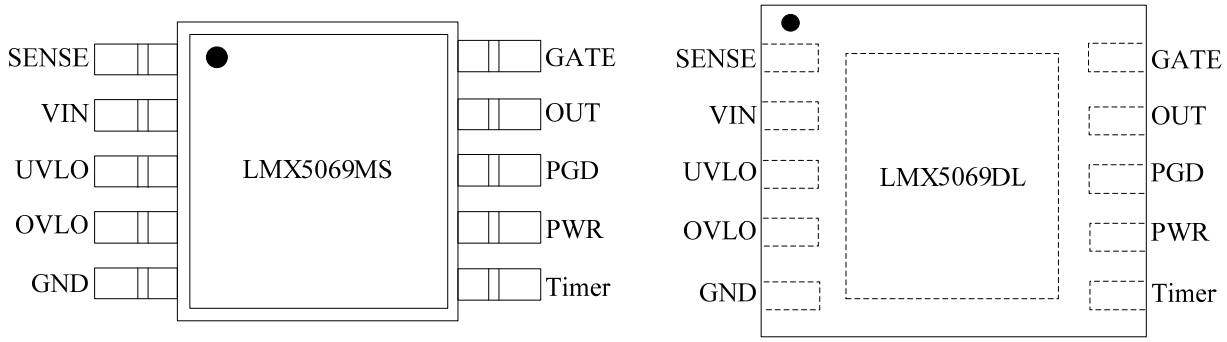
Symbol	Range
Supply voltage	9 to 90V
OVP, PWR, Timer voltage	0 to 5V
Junction temperature	-40 to 125℃

Typical application



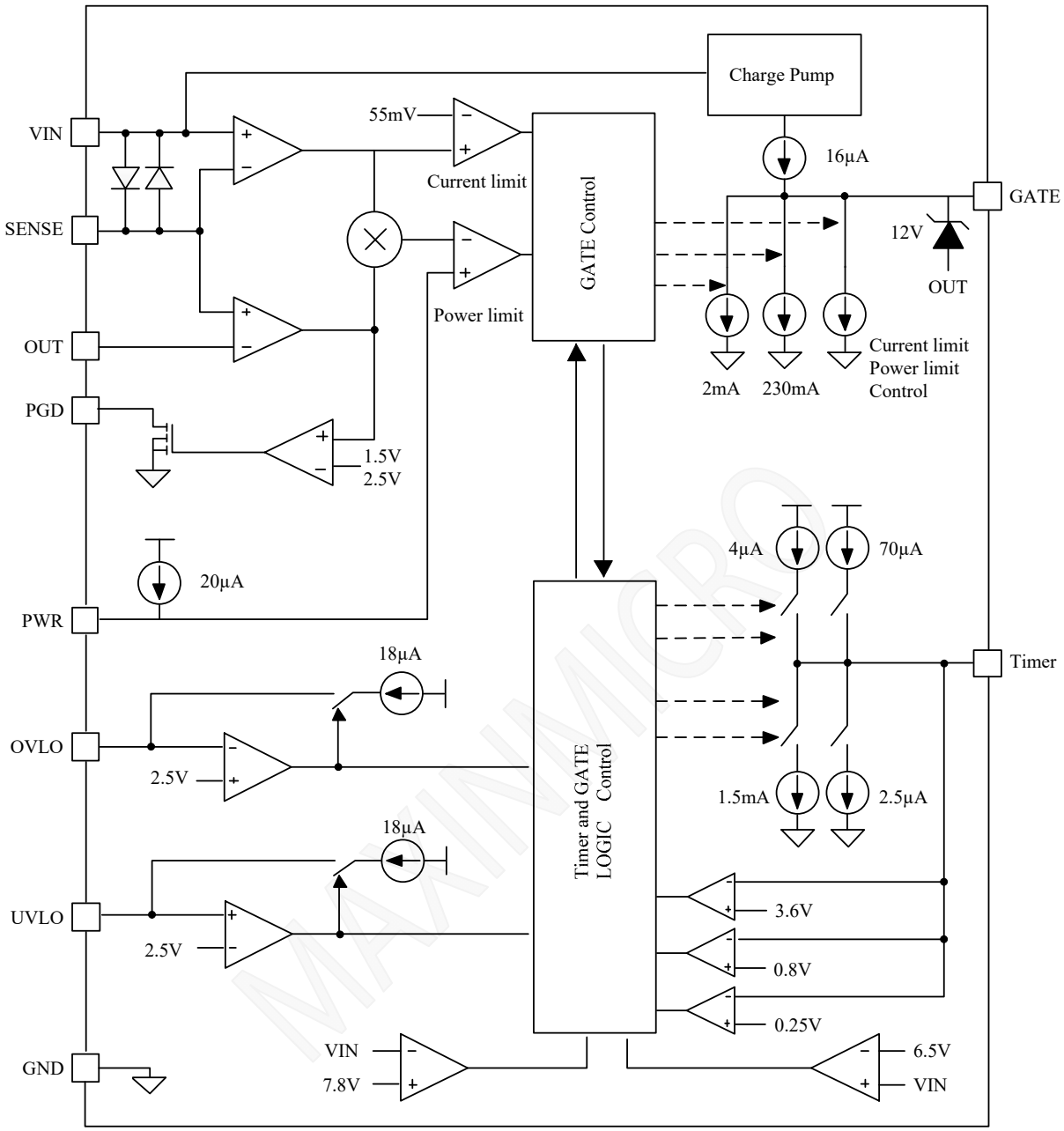


Terminal assignments



PIN num	PIN name	Description
1	SENSE	Current sense input: The voltage across the current sense resistor (RS) is measured from VIN to this pin. If the voltage across the RSENSE reaches 55mV the load current is limited and the fault timer activates.
2	VIN	Positive supply input: A small ceramic bypass capacitor close to this pin is recommended to suppress transients which occur when the load current is switched off.
3	UVLO	This is a dual function control pin. When used as an ENABLE pin and pulled down, it shuts off the internal pass MOSFET. As an UVLO pin, it can be used to program different UVLO trip point via external resistor divider.
4	OVLO	Overvoltage lockout: An external resistor divider from the system input voltage sets the overvoltage turnoff threshold. An internal 18μA current source provides hysteresis. The disable threshold at the pin is 2.5V typical.
5	GND	Circuit ground
6	Timer	Timing capacitor: An external capacitor connected to this pin sets the insertion time delay and the fault timeout period. The capacitor also sets the restart timing.
7	PWR	Current limit set: An external resistor connected to this pin, in conjunction with the current sense resistor, sets the maximum power dissipation allowed in the external series pass MOSFET.
8	PGD	Power Good indicator: An open drain output. When the external MOSFET VDS decreases below 1.5 V, the PGD indicator is active. When the external MOSFET VDS increases above 2.5V the PGD indicator switches low.
9	OUT	Output feedback: Connect to the output rail (external MOSFET source). Internally used to determine the MOSFET VDS voltage for power limiting, and to control the PGD indicator.
10	GATE	Gate drive output: Connect to the external MOSFET's gate. This pin's voltage is typically 12V above the OUT pin when enabled.
11	Thermal PAD	Ground

Block diagram



Electrical characteristics

VIN = 24-48V, T_J = 25°C, unless otherwise noted.

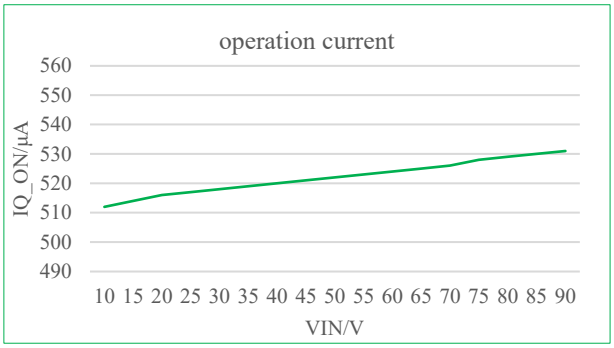
Symbol	Parameters	Test conditions	Min	Typ	Max	Unit
INPUT (VIN PIN)						
VIN			8		90	V
IQ_{ON}	Supply current	UVLO>2.5V and OVLO<2.5V	300		650	μA
IQ_{OFF}		UVLO<2.5V	100		350	μA
V_{INSERT}			5.5	6.5	7.5	V
V_{INEN}			6.8		8.5	V
UVLO						
V_{UVLOR}	UVLO Threshold voltage	falling	2.25	2.5	2.75	V
$UVLO_{HYS}$	UVLO hysteresis current	UVLO=1V	12	18	24	μA
$UVLO_{BIAS}$	UVLO bias current	UVLO=48V			1	μA
OVLO						
V_{OVLOR}	OVLO Threshold voltage	Rising	2.25	2.5	2.75	V
$OVLO_{HYS}$	OVLO hysteresis current	OVLO=3V	12	18	24	μA
$OVLO_{BIAS}$	OVLO bias current	OVLO=2V			1	μA
OUT PIN						
I_{OUT_DIS}	OUT bias current, disabled	Disabled, OUT = 0V, SENSE = VIN		50		μA
I_{OUT_EN}	OUT bias current, enabled	Enabled, OUT=VIN		11		μA
GATE CONTROL (GATE PIN)						
I_{GATE}	Source current	Normal operation	10	15	22	μA
	Sink current	UVLO < 2.5V	1.7	2	2.5	mA
		VIN to SENSE = 150mV, GATE=5V	45	230	300	mA
V_{GATE}	Gate output voltage in normal	GATE-OUT voltage	10		14	V
PWR						
PWR_{ILM-1}	Power limit sense voltage (VIN-SENSE)	SEN-OUT=48V，RPWR=150kΩ	19	25	31	mV
PWR_{ILM-2}		SENSE-OUT=24V，RPWR=75 kΩ		25		mV
I_{PWR}	Power pin current	PWR=2.5V	17	20	23	μA
CURRENT LIMIT						
V_{CL}	Over current threshold	VIN-VSENSE	48	55	65	mV
I_{SENSE}	SENSE input current	Enable, OUT=SENSE		8		μA
		Disable, OUT=0V		10		μA
CIRCUIT BREAKER						
V_{CB}	Threshold voltage	VIN to SENSE	80	105	130	mV
TIMER						
V_{TMRH}	Upper threshold	End of insertion time	3.2	3.6	4.0	V
V_{TMRL}	Lower threshold	Restart cycles	0.5	0.8	1.1	V
		End of 8th cycles		0.25		V
I_{TIMER}	Insertion time current	VIN=V_{INSERT}	2	4	6	μA
	Sink current, end of insertion time	Timer=2V	0.7		2	mA
	Fault detection current		45	70	95	μA
	Fault sink current		1.25	2.5	3.75	μA
DT_{FAULT}	Fault restart duty cycle			0.5		%
PGD						
PGD_{TH}	Threshold at SENSE-OUT	Decreasing	0.6	1.5	2.5	V
		Increasing, relative to decreasing threshold	0.3	1.25	1.5	V

PGD_{VOL}	Output low voltage	I_{SINK}=2mA		60	150	mV
PGD_{IOH}	Off leakage current	V_{PGD}=80V			5	μA

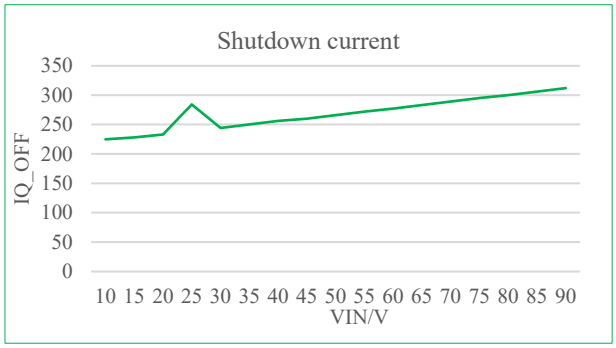
Timing characteristics

OVLO Timing						
$UVLO_{DLY}$	UVLO delay	UVLO rising to GATE begin to rise		55		μs
		UVLO falling to GATE begin to fall		20		μs
OVLO Timing						
$OVLO_{DLY}$	OVLO delay	OVLO rising to GATE begin to fall		20		μs
		OVLO falling to GATE begin to rise		55		μs
Current Limit and Circuit Breaker Timing						
T_{CL}	Response time for OCP	VIN-SENSE stepped from 0V to 80mV		50		μs
T_{CB}	Response time	VIN-SENSE stepped from 0V to 150mV, time to GATE low, no load		1		μs
Fault Timing						
t_{FAULT}	Fault to GATE low delay	Timer pin reaches 3.6V		12		μs

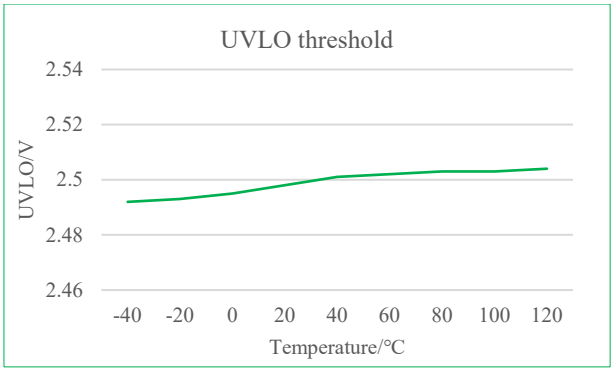
Characteristic plot



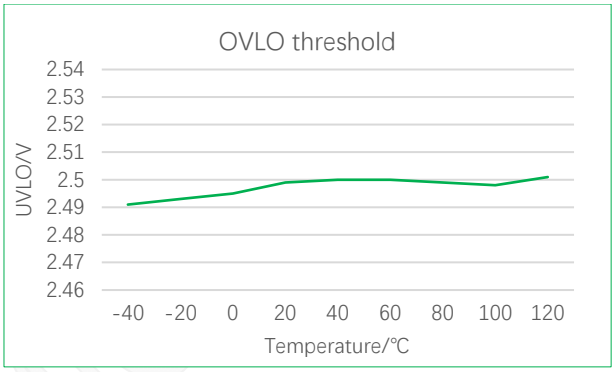
The operation current vs input voltage



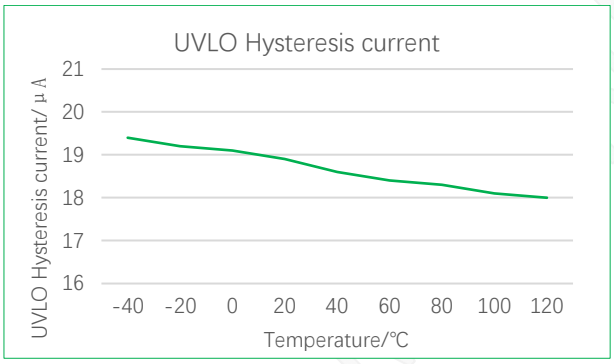
The shotdown current vs input voltage



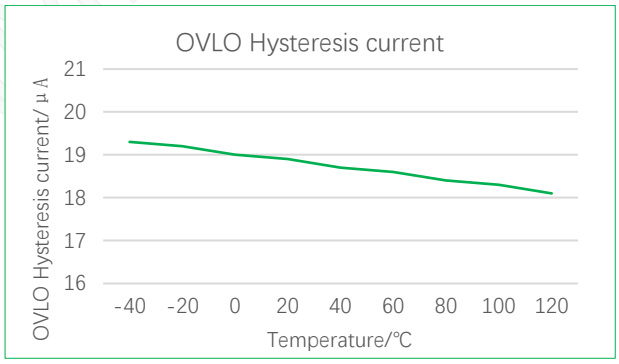
UVLO threshold vs temperature



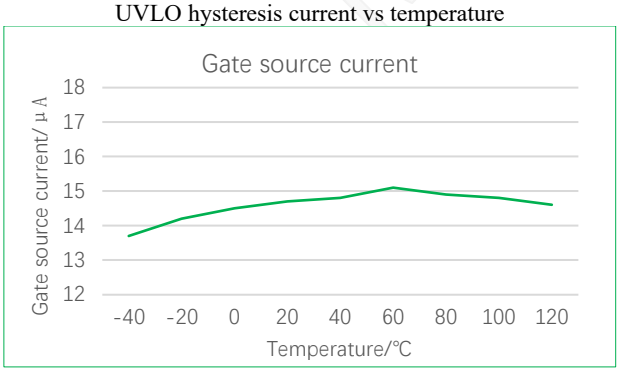
OVLO threshold vs temperature



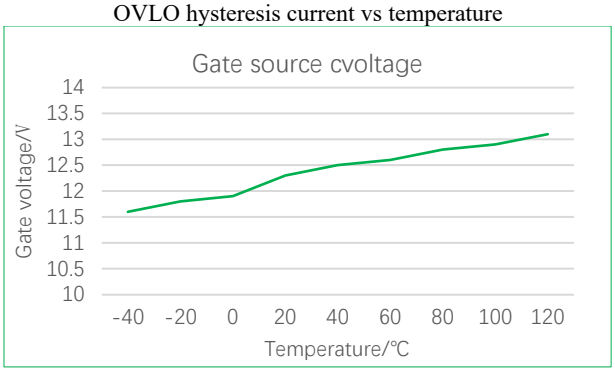
UVLO hysteresis current vs temperature



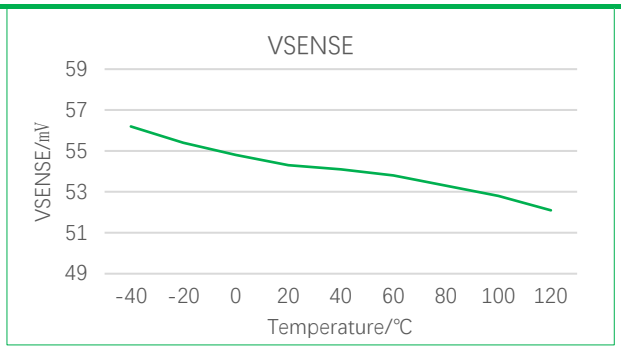
OVLO hysteresis current vs temperature



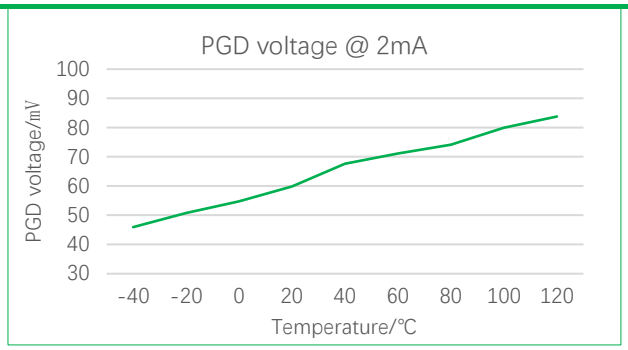
GATE source current vs temperature



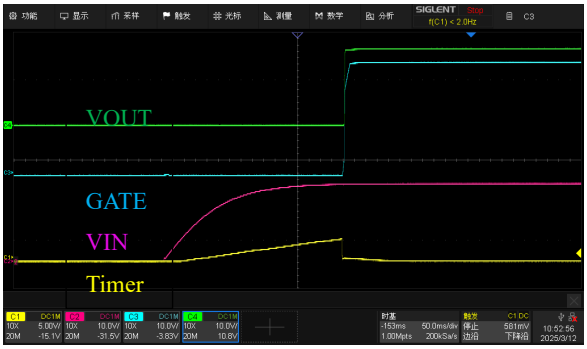
GATE to source voltaget vs temperature



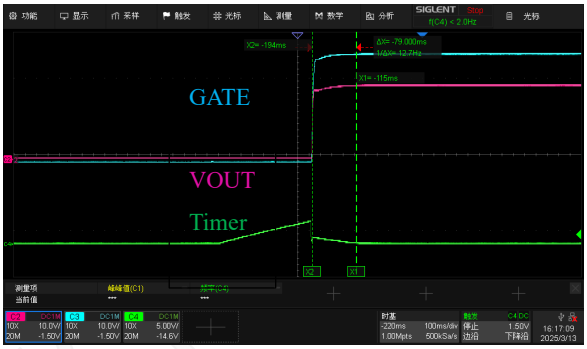
Current limit sense voltage vs temperature



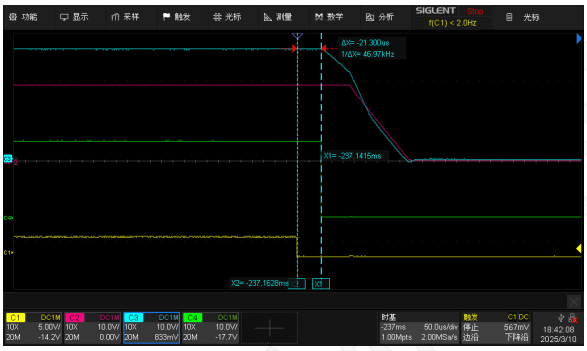
The PGD voltage vs temperature



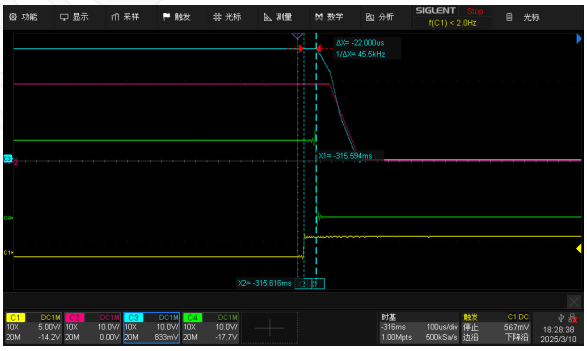
Insertion time when Timer pin capacitor is 150nF



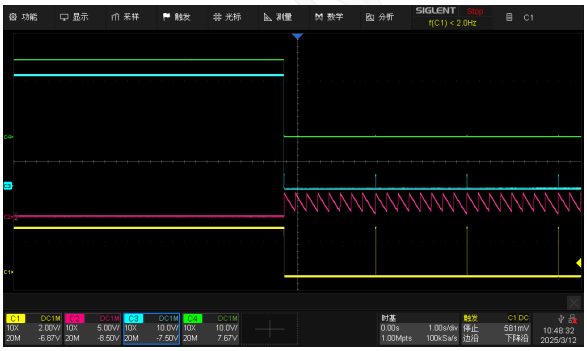
Start timing with output capacitor1000uF



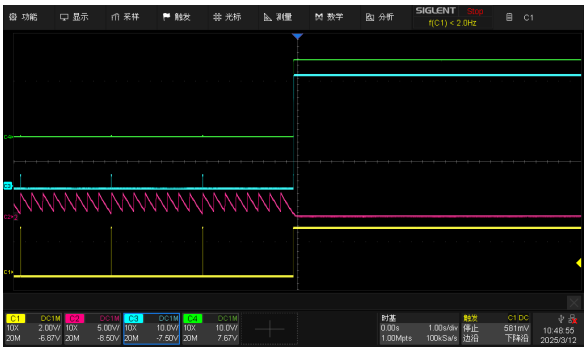
UVLO protection



OVLO protection

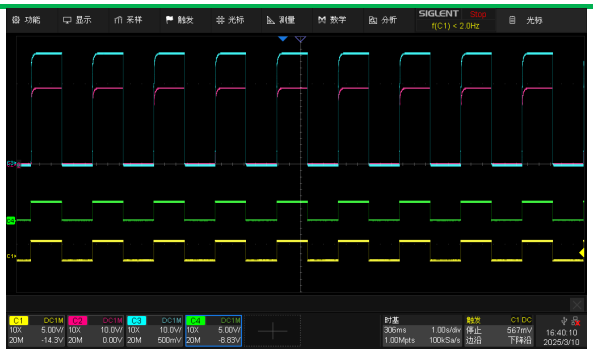


Over current protection



Over current release

Short circuit protection



Continues repeated switch on an off with 10A load

Detailed description

Overview

LMX5069 have programmable current limit, current limiting for an extended period results in the shutdown of the series pass device. In this event, the LMX5069 retries an infinite number of times to recover after the fault is removed. The circuit breaker function quickly switches off the series pass device upon detection of a severe overcurrent condition. Programmable undervoltage lockout (UVLO) and overvoltage lockout (OVP) circuits shut down the LMX5069 when the system input voltage is outside the desired operating range.

In addition to a programmable current limit, the LMX5069 monitors and limits the maximum power dissipation in the series pass device to maintain operation within the device Safe Operation Area. Either current limiting or power limiting for an extended period of time results in the shutdown of the series pass device. In this event, the LMX5069 retries an infinite number of times to recover after the fault is removed. The circuit breaker function quickly switches off the series pass device upon detection of a severe overcurrent condition.

Undervoltage Lockout (UVLO)

The series pass MOSFET is enabled when the input supply voltage is within the operating range defined by the programmable undervoltage lockout and overvoltage lockout levels. Typically, the UVLO level at VIN is set with a resistor divider as shown in the figure below. When VIN is below the UVLO level, the internal 18 μ A current source at UVLO is enabled, the current source at OVLO is off, and Q1 is held by 1mA pulldown current at the GATE pin. As VIN is increased, raising the voltage at UVLO above 2.5V, the 18 μ A current source at UVLO is switched off, increasing the voltage at UVLO, providing hysteresis for this threshold. With the UVLO pin above 2.5V, Q1 is switched on by 16μA current source at the GATE pin if the insertion time delay has expired.

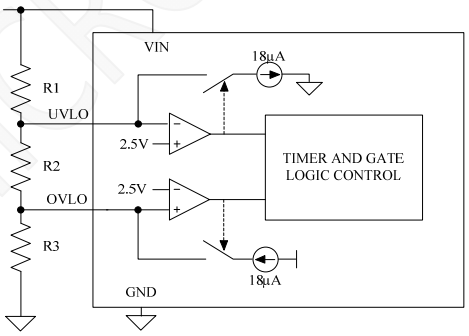
The minimum possible UVLO level at VIN can be set by connecting the UVLO pin to VIN. In this case Q1 is enabled when the VIN voltage reaches the V_{INEN} threshold.

By programming the UVLO and OVLO threshold the LMX5069 enables the pass series MOSFET when the input supply voltage is within the desired operational range. If VIN is below the UVLO threshold, or above the OVLO threshold, Q1 is switched off, denying power to the load. Hysteresis is provided for each threshold.

There are four methods to configure UVLO and OVLO to set the hysteresis threshold.

Option A

The configuration shown in the following figure requires three resistors (R1-R3) to set the threshold.



The procedure to calculate the resistor values is as follows:

1. Choose the upper UVLO threshold (V_{UVH}), and the lower UVLO threshold (V_{UVL}).
2. Choose the upper OVLO threshold (V_{OVH}).
3. The lower OVLO threshold (V_{OVL}) cannot be chosen in advance in this case but is determined after the values for R1-R3 are determined.

The resistors are calculated with Equation1, Equation2 and Equation3.

$$R1 = \frac{V_{UVH}-V_{UVL}}{18\mu A} = \frac{V_{UV(HYS)}}{18\mu A} \quad (1)$$

$$R3 = \frac{2.5\times R1\times V_{UVL}}{V_{OVH}\times(V_{UVL}-2.5V)} \quad (2)$$

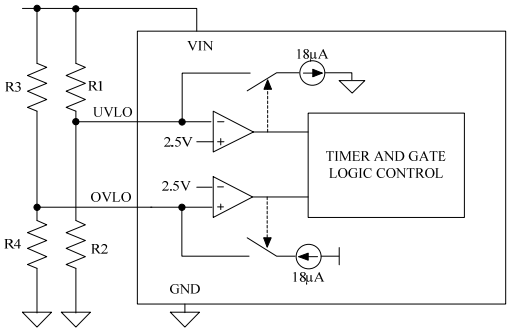
$$R2 = \frac{2.5V\times R1}{V_{UVL}-2.5V} - R3 \quad (3)$$

The lower OVLO threshold is calculated from Equation4.

$$V_{OVL} = \left[(R1 + R2) \times \left(\frac{2.5V}{R3} - 18\mu A\right)\right] + 2.5V \quad (4)$$

Option B

If all four thresholds must be accurately defined, the following figure can be used.



The four resistor values are calculated as follows:

1. Choose the upper UVLO threshold (V_{UVH}) and lower UVLO threshold (V_{UVL}) with Equation5 and Equation6.

$$R1 = \frac{V_{UVH} - V_{UVL}}{18\mu A} = \frac{V_{UV(HYS)}}{18\mu A} \quad (5)$$

$$R2 = \frac{2.5V \times R1}{V_{UVL} - 2.5V} \quad (6)$$

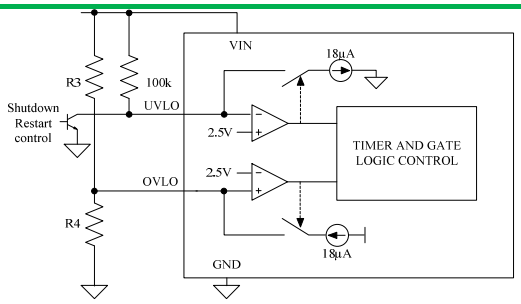
2. Choose the upper OVLO threshold (V_{OVH}) and lower OVLO threshold (V_{OVL}) with Equation7 and Equation8.

$$R3 = \frac{V_{OVH} - V_{OVL}}{18\mu A} = \frac{V_{OV(HYS)}}{18\mu A} \quad (7)$$

$$R4 = \frac{2.5V \times R3}{V_{OVH} - 2.5V} \quad (8)$$

Option C

The minimum UVLO level is obtained by connecting the UVLO pin to VIN as shown in the following figure. Q1 is switched on when the VIN voltage reaches V_{INEN} threshold. An external transistor can be connected to UVLO to provide remote shutdown control. The OVLO threshold is set using R3, R4. Their values are calculated using the method in Option B.



Option D

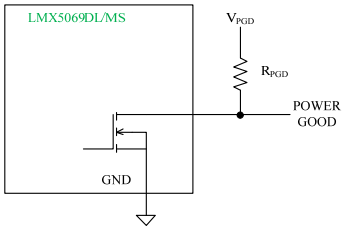
The OVLO function can be disabled by grounding the OVLO pin. The UVLO thresholds are set as described in Option B and Option C.

Overvoltage Lockout (OVLO)

The series pass MOSFET is enabled when the input supply voltage is within the operating range defined by the programmable undervoltage lockout and overvoltage lockout level. If VIN raises the OVLO pin voltage above 2.5V, Q1 is switched off by 2mA pulldown current at the GATE pin, denying power to the load. When the OVLO pin is above 2.5V, the internal 18 µ A current is reduced below the OVLO level Q1 is enabled.

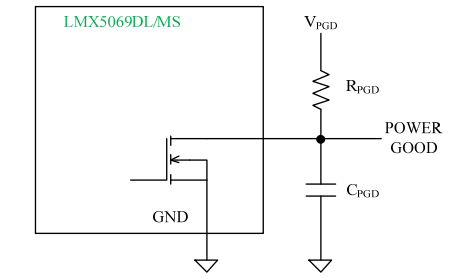
Power Good Pin

During turn-on, the Power Good pin (PGD) is high until the voltage at VIN increases above 5V. PGD then switches low, remaining low as the VIN voltage increases. When the voltage at OUT increases to within 1.5V of the SENSE pin (VDS <1.5V), PGD switches high. PGD switches low if the VDS of Q1 increases above 2.5V. A pullup resistor is required at PGD as shown in the following figure. The pullup voltage (VPGD) can be as high as 80V and can be higher and lower than the voltage at VIN and OUT.

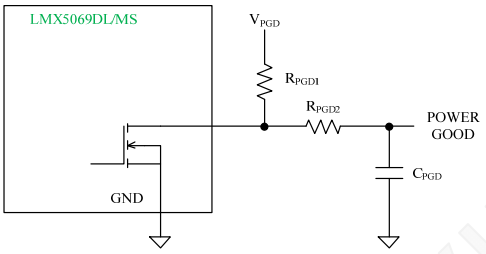


Power Good Output

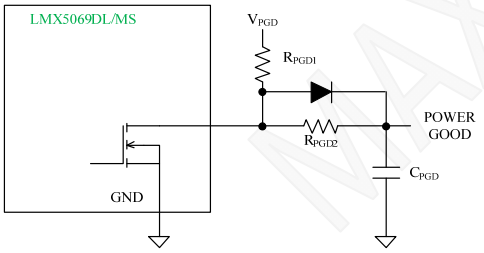
If a delay is required at PGD, suggested circuits are shown in the following figure. In figure a), capacitor C_{PG} adds delay to the rising edge, but not to the falling edge. In figure b), the rising edge is delayed by R_{PGD1} + R_{PGD2} and C_{PG}, while the falling edge is delayed by a lesser amount by R_{PG2} and C_{PGD}. In figure c), adding a diode across R_{PG2} allows for equal delays at the two edges, or a short delay at the rising edge and a long delay at the falling edge.



a) Delay Rising Edge Only



b) Long delay at rising edge, short delay at falling edge



c) Short Delay at Rising Edge and Long Delay at Falling Edge or Equal Delays

Adding delay to the power good output pin

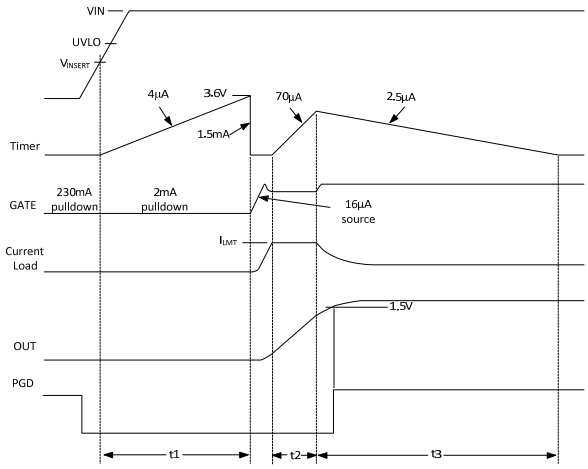
Power up sequence

The VIN operating range of the LMX5069 is 9V to 80V, with a transient capability to 100V. As the VIN initially increases, the external NMOSFET is held off by an 230mA pulldown current at the GATE pin. The strong pulldown current at the GATE pin prevents an inadvertent turn on as the MOSFET's gate to drain capacitance is charged. Additionally, the Timer pin is initially held at ground. When the VIN voltage reaches the VINSERT threshold the insertion time begins. During the insertion time, the capacitor at the Timer pin is charged by a 4μA current source, and Q1 is held off by a 2mA pulldown current at the GATE pin regardless of the VIN voltage. The insertion time delay allows ringing and transient at VIN to settle before Q1 can be enabled.

The insertion time ends when the Timer pin voltage reaches 3.6V. The capacitor is the quickly discharged by an internal 1.5mA pulldown current. After the insertion time, the LMX5069 control circuity is enabled when VIN reaches the VINEN threshold. The GATE pin then switches on Q1 when VIN exceeds the UVLO threshold. If VIN is above the UVLO threshold at the end of the insertion time, Q1 switches on at that time. The GATE pin charge pump sources 16μA to charge Q1'S gate capacitance. The maximum gate to source voltage of Q1 is limited by an internal 12V Zener diode.

As the voltage at the OUT pin increases, the LMX5069 monitors the drain current and power dissipation of MOSFET. Inrush current limiting and power limiting circuits actively control the current delivered to the load. During the inrush limiting interval an internal 70μA fault timer current source charges the timer capacitor. If Q1's power dissipation and the input current reduce below their respective limiting threshold before the Timer pin reaches 3.6V, the current 70μA source is switched off, and the capacitor is discharged by the internal 2.5μA current sink. The in rush limiting interval is complete when the voltage at the OUT pin increases to within 1.5V of the input voltage, and the PGD pin switches high.

The Timer pin voltage 3.6V before in rush current limiting or power limiting ceases, a fault is declared and Q1 is turned off.



Gate control

A charge pump provides internal bias voltage above the output voltage (OUT pin) to enhance the N-Channel MOSFET's gate. The gate-to-source voltage is limited by an internal 12V Zener diode. During normal operating conditions the gate of Q1 is held charged by an internal 16µA current source to approximately 12V above OUT.

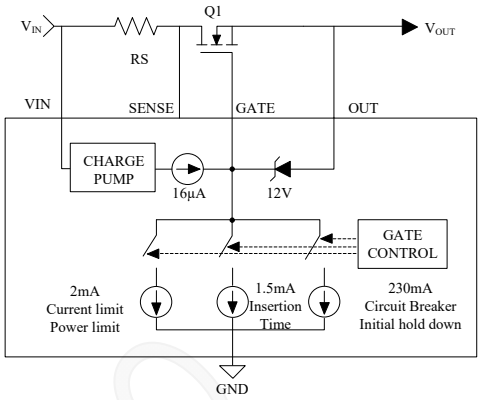
When the system voltage is initially applied, the GATE pin is held low by a 230mA pulldown current. This helps prevent an inadvertent turn on of the MOSFET through its Miller capacitor as the applied system voltage increases.

During insertion time the GATE pin is held low by a 2mA pulldown current. This maintains the MOSFET in the off state until the end of t1, regardless of the voltage at VIN or UVLO.

Following the insertion time, during t2 in the above figure, the gate voltage of Q1 is modulated to keep the current or power dissipation level from exceeding the programmed levels. While in the current or power limiting mode the Timer capacitor is charging. If the current and power limiting cease before the Timer pin reaches 3.6V the Timer pin capacitor then discharges, and the circuit enters normal operation.

If the inrush limiting condition persists such that the Timer pin reached 3.6Vduring t2, the GATE pin is then pulled low by 2mApulldown current. The GATE pin is then held low until then end of the restart sequence.

If the system input voltage falls below the UVLO threshold, or rises above the OVLO threshold, the GATE pin is pulled low by the 2mA pulldown current to turn off the MOSFET.

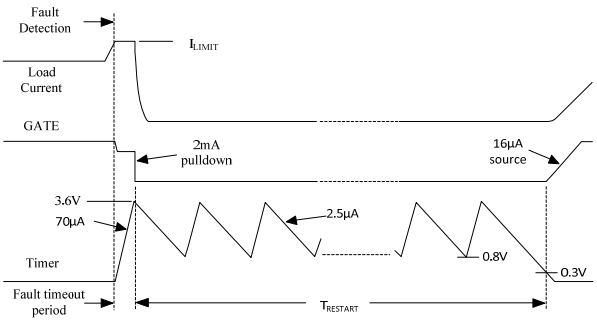


Fault timer and restart

When the current limit or power limit threshold is reached during turn on or as result of a fault condition, the gate to source voltage is modulated to regulate the load current and power dissipation. When either function is activated, an 70µA fault timer current source charged the external capacitor at the Timer pin. If the fault condition subsides during the fault timeout period before the Timer pin reaches 3.6V, the LMX5069returns to the normal operating mode and the Timer capacitor is discharged by the 2.5µA current sink. If the Timer pin reaches 3.6V during the fault timeout period, MOSFET is switched off by 2mA pulldown current at the GATE pin.

The LMX5069 provides an automatic restart sequence which consists of the Timer pin cycling between 3.6V and 0.8V seven times after the fault timeout period as shown in the following figure. The period of each cycle is determined by the 70µA charging current, and the 2.5µA discharging current, and the value of the capacitor at Timer pin. When the Timer pin reaches 0.3V during the eight high to low ramp, the 16µA current source at the GATE pin turns on the

MOSFET. If the fault condition is still present, the fault timeout period and the restart cycle repeat.



The fault timer runs when the hot swap is in power limit or current limit, which is the case during start up. Thus, the timer has to be sized large enough to prevent a time out during start up. If the part starts directly into current limit the maximum start time can be computed with Equation9.

$$t_{start,max} = \frac{C_{OUT} \times V_{INMAX}}{I_{LIM}} \quad (9)$$

For most designs, $I_{LIM} \times V_{DS} > P_{LIM}$, so the hot swap starts in power limit and transition into current limit. In that case, the estimated start time can be computed with Equation10.

$$t_{start} = \frac{C_{OUT}}{2} \times \left(\frac{V_{INMAX}^2}{P_{LIM}} + \frac{P_{LIM}}{I_{LIM}^2}\right) \quad (10)$$

Note that the above start time assumes constant, typical current limit and power limit values. The actual start up time is slightly longer, as the power limit is a function of VDS and decreases as the output voltage increases. To ensure that the timer never times out during start up, we recommend setting the minimum fault time to be greater than the startup time by adding an additional 50% of the fault time. This accounts for the variation in power limit, timer current and timer capacitance. Thus, the charge time can be computed with Equation11.

$$t_{FLT} = \frac{C_{Timer} \times 3.6V(typ)}{70\mu A(typ)} \quad (11)$$

Current Limit

The current limit threshold reached when the voltage across the sense resistor R_S (VIN to SENSE) reaches 55mV. In the current limiting condition, the GATE voltage is controlled to limit the current in MOSFET Q1. While the current limit circuit is active, the fault SST is active. If the load current falls below the current limit threshold before the end of the fault timeout period. For proper operation, the RS resistor value must be no larger than 100mΩ.

Circuit breaker

If the load current increases rapidly (for example, the load is short-circuited) the current in the sense resistor (RS) may exceed the current limit threshold before the current limit control loop is able to respond. If the current exceeds twice the current limit threshold (105mV/RS), Q1 is quickly switched off by the 230mA pulldown current at the GATE pin, and a fault timeout period begins. When the voltage across RS falls below 105 mV the 230mA pulldown current at the GATE pin is switched off, and the gate voltage of Q1 is then determined by the current limit or the power limit functions. If the TIMER pin reaches 3.6V before the current limiting or power limiting condition ceases, Q1 is switched off by the 2 mA pulldown current at the GATE pin.

Power limit

An important feature of the LMX5069 is the MOSFET power limit. The power limit function can be used to maintain the maximum power dissipation of MOSFET Q1 within the device SOA rating. The LMX5069 determines the power dissipation in Q1by monitoring its drain to source voltage, and the drain current through the sense resistor. The product of the current and voltage is compared to the power limit threshold programmed by the resistor at the PWR pin. If the power dissipation reaches the limiting circuit is active.

In general, a lower power limit setting is preferred to reduce the stress on the MOSFET. However, when the LMX5069 is set to a very low power limit setting, it must regulate the FET current and hence the voltage across the sense resistor to a

very low value. V_{SENSE} can be computed as shown in Equation12.

$$V_{SENSE} = \frac{P_{LIM} \times R_{SENSE}}{V_{DS}} \quad (12)$$

To avoid significant degradation of the power limiting accuracy, a V_{SENSE} of less than 5mV is not recommended. Based on this requirement the minimum allowed power limit can be computed in Equation13.

$$P_{ILIMMIM} = \frac{V_{SENSEMIN} \times V_{INMAX}}{R_{SENSE}} = \frac{5mV \times V_{INMAX}}{R_{SENSE}} \quad (13)$$

Note that the minimum R_{PWR} would occur when $V_{DS}=V_{INMAX}$. We can then compute the minimum R_{PWR} with Equation14.

$$R_{PWR} = 180000 \times R_{SENSE} \left(P_{LIM} - 1.0mV \times \frac{V_{INMAX}}{R_{SENSE}} \right) \quad (14)$$

Input and Output Protection

Proper operation of the LMX5069 hot swap circuit requires a voltage clamping element present on the supply side of the connector into which the hot swap circuit is plugged in. A TVS is ideal, as depicted in Typical application. The TVS is necessary to absorb the voltage transient generated whenever the hot swap circuit shuts off the load current. This effect is the most severe during a hot-short when a large current is suddenly interrupted when the FET shuts off. The TVS must be chosen to have minimal leakage current at V_{INMAX} and to clamp the voltage to under 30V during hot-short events. A 100~200ohm resistor should be palced between OUT pin and Source of external MOSFET to prevent damage from surge voltage, as the R_{SOURCE} shown in the Typical application.

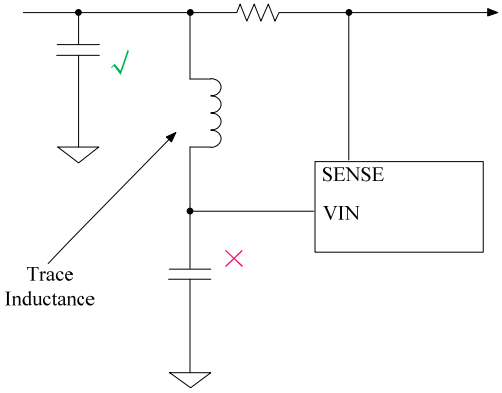
Power Supply Recommendations

In general, the LMX5069 behavior is more reliable if it is supplied from a very regulated power supply. However, high-frequency transients on a backplane are not uncommon due to adjacent card insertions or faults. If this is expected in the end system, Maxin recommends placing a 1μF ceramic capacitor to ground close to the drain of the hot swap MOSFET. This reduces the common mode voltage seen by VIN and SENSE. Additional filtering may be necessary to avoid nuisance trips.

Layout Guidelines

The following guidelines must be followed when designing the PC board for the LMX5069:

- Place the LMX5069 close to the board's input connector to minimize trace inductance from the connector to the FET.
- Note that special care must be taken when placing the bypass capacitor for the VIN pin. During hot shorts, there is a very large dv/dt on input voltage after the MOSFET turns off. If the bypass capacitor is placed right next to the pin and the trace from R_{SENSE} to the pin is long, an LC filter is formed. As a result, a large differential voltage can develop between VIN and SENSE. To avoid this, place the bypass capacitor close to R_{SENSE} instead of the VIN pin.



Layout Trace Inductance

- The sense resistor (R_S) must be close to the LMX5069, and connected to it using the Kelvin techniques.
- The high current path from the board's input to the load (via Q1), and the return path, must be parallel and close to each other to minimize loop inductance.
- The ground connection for the various components around the LMX5069 must be connected directly to each other,

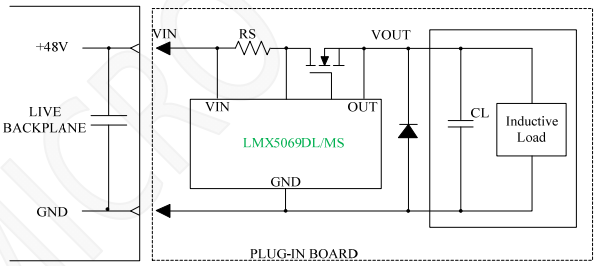
and to the LMX5069's GND pin, and then connected to the system ground at one point. Do not connect the various component grounds to each other through the high current ground line.

- Provide adequate heat sinking for the series pass device (Q1) to help reduce stresses during turn on and turn off.
- The board's edge connector can be designed to shut off the LMX5069 as the board is removed, before the supply voltage is disconnected from the LMX5069. When the board is inserted into the edge connector, the system voltage is applied to the LMX5069's VIN pin before the UVLO voltage is taken high.

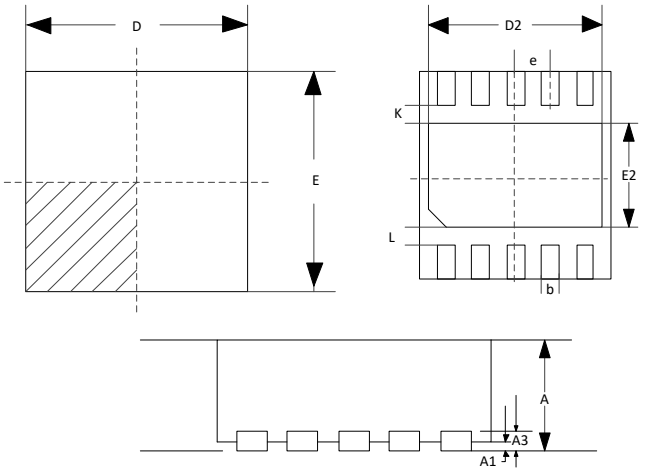
System Considerations

A) Continued proper operation of the LMX5069 hot swap circuit requires capacitance to be present on the supply side of the connector into which the hot swap circuit is plugged in, as depicted in the following figure. The capacitor in the Live Backplane section is necessary to absorb the transient generated whenever the hot swap circuit shuts off the load current. If the capacitance is not present, inductance in the supply lines generates a transient voltage at shut-off which can exceed the absolute maximum rating of the LMX5069, resulting in its destruction.

B) If the load powered via the LMX5069 hot swap circuit has inductive characteristics, a diode is required across the LMX5069's output. The diode provides a recirculating path for the load's current when the LMX5069 shuts off that current. Adding the diode prevents possible damage to the LMX5069 as the OUT pin is taken below ground by the inductive load at shutoff.



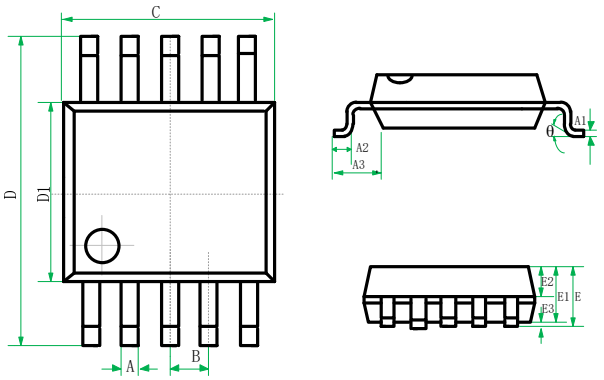
Package information DFN3*3-10L



DFN3*3-10L for LMX5069DL

SYMBOL	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.70	0.75	0.80	0.0275	0.0295	0.0315
A1	0.00	0.03	0.05	0.00	0.0012	0.0020
A3		0.20BSC			0.008BSC	
b	0.18	0.24	0.30	0.007	0.009	0.011
D		3.00BSC			0.12BSC	
D2	2.45	2.50	2.55	0.096	0.098	0.100
E		3.00BSC			0.12BSC	
E2	1.75	1.80	1.85	0.069	0.071	0.073
e		0.50BSC			0.02BSC	
K		0.19TYP			0.0075BSC	
θ	0.35	0.40	0.45	0.014	0.016	0.018

Package information MSOP -10L



MSOP10L for LMX5069MS

SYMBOL	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.18		0.26	0.007		0.010
A1	0.15		0.19	0.0060		0.0075
A2	0.40		0.70	0.016		0.027
A3	0.05		0.15	0.002		0.006
B		0.50BSC			0.02BSC	
C	2.90	3.00	3.10	0.114	0.118	0.122
D	4.70	4.90	5.10	0.185	0.193	0.210
D1	2.90	3.00	3.10	0.114	0.118	0.122
E			1.10			0.043
E1	0.75	0.85	0.95	0.030	0.033	0.037
E2	0.30	0.35	0.40	0.012	0.014	0.016
E3	0.05		0.15	0.002		0.006
θ	0°		8°			

Restrictions on Product Use

◆ MAXIN micro is continually working to improve the quality and reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing MAXIN products, to comply with the standards of safety in making a safe design for the entire system, and to avoid situations in which a malfunction or failure of such MAXIN products could cause loss of human life, bodily injury or damage to property.

◆ In developing your designs, please ensure that MAXIN products are used within specified operating ranges as set forth in the most recent MAXIN products specifications.

◆ The information contained herein is subject to change without notice.

Version update record:

V10 The original version （preliminary）

V11 Change the Marking information

V12 Updated Package information of DFN3*3-10L

V13 Add the description of the Circuit Breaker.