

GENERAL DESCRIPITION

The MX3502S of push pull output comparator feature a fast 5ns propagation delay and operation from 1.8V to 5.5V. Beyond the rails input common-mode range makes it an ideal choice for low voltage applications. The rail to rail output directly drives either CMOS or TTL logic.

Micro-size package provide option for portable and space restricted applications. The single is available in SOP8L.

FEATURES

♦ High Speed: 5ns typical

♦ Rail to Rail I/O

♦ Supply Voltage: 1.8V to 5.5V

♦ Push Pull CMOS Output Stage

♦ Shutdown

♦ Low Supply Current: 3.2mA

♦dual channel 8-Pin SOP8L Package

APPLICATIONS

Test equipment

Wireless base stations Threshold detectors Zero crossing detectors Window comparators Test equipment

GENERAL INFORMATION

Ordering information

Part Number	Description	MPQ
MX3502S	SOP8L	3K

Package dissipation rating

2	
Package	RθJA (°C/W)
SOP8L	90

Absolute maximum ratings

Parameter	Value
Supply voltage	-0.7to 6V
IN+、IN- signal pin voltage	(V-)-0.3 to
	(V+)+0.3
IN+、IN- signal pin current	10mA max
OUT pin short circuit	70mA
Junction temperature	150°C
Storage temperature, Tstg	-55 to 150°C
Leading temperature (soldering,	260℃
10secs)	200 C
ESD Susceptibility HBM	±2000V

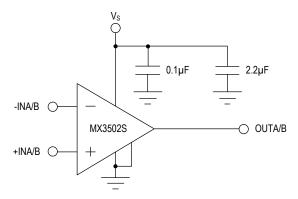
Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

Recommended operating condition

Symbol	Parameter	Range
Supply	Supply voltage	2.7-5.5V
Junction		-40~125°C
temperature		
PD	Power dissipation	0.50W

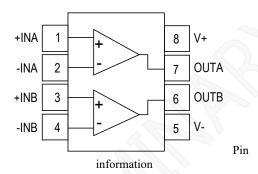


TYPICAL APPLICATION



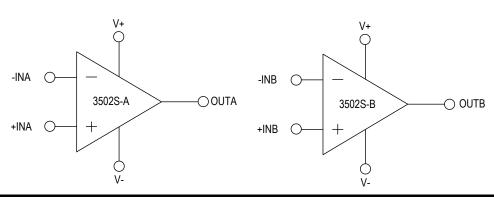
Basic connections for the MX3502S

TERMINAL ASSIGMENTS



PIN NO.	PIN name	Description	
1	+INA	A channel positive (noninverting) input	
2	-INA	A channel negative (inverting) input	
3	+INB	B channel positive (noninverting) input	
4	-INB	B channel negative (inverting) input	
5	V-	Negative (lowest) power supply	
6	OUTB	B channel output	
7	OUTA	A channel output	
8	V+	Positive (highest) power supply	

BLOCK DIAGRAM





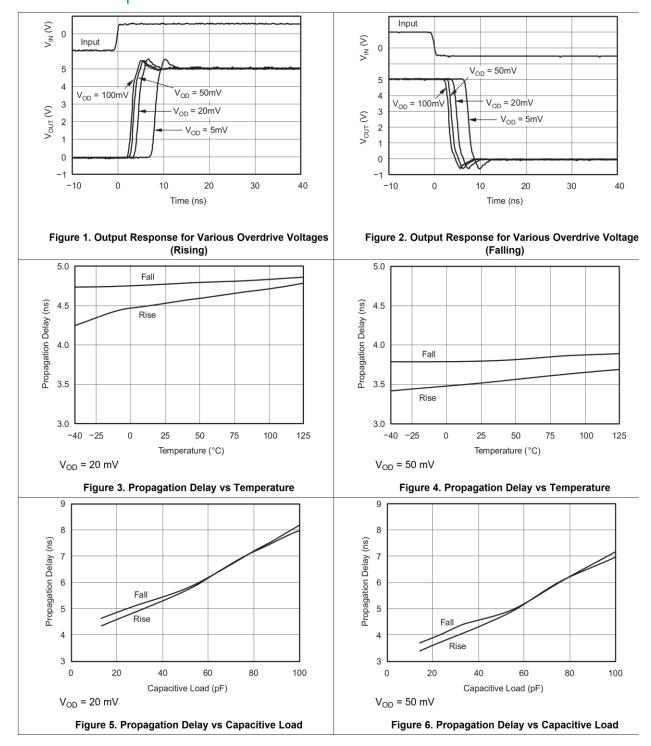
Electrical characteristics

(TA=25°C, VDD=2.7-5.5V, unless otherwise noted)

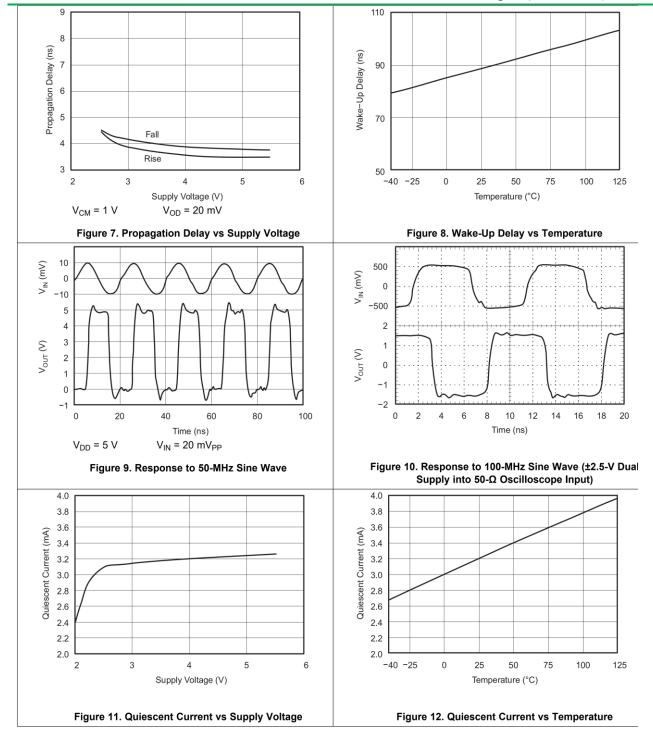
Symbol	Parameter	Test condition	Min	Тур.	Max	Unit
OFFSET VOLTAGE						
Input offset voltage	Vos	VCM=0V, IO=0mA		±1	±6.5	mV
Input offset voltage vs	dVos/dT	TA=-40°C to +125°C		±5		μV/°C
temperature	u v os/ur	1A40 C to +123 C		<u> </u>		μ ν / С
Input offset voltage vs power	PSRR	VS=1.8V to 5.5V		100	400	μV/V
supply	Total	V 5 1.0 V 10 5.5 V			100	μνν
Input hysteresis				6		mV
INPUT BASIC CURENT	ı			<u> </u>	1	
Input basic current	I_{B}	VCM=VCC/2		±2	±10	pA
Input offset current	Ios	VCM=VCC/2		±2	±10	pA
INPUT VOLTAGE RANGE	I		- N			
Common mode voltage range			(V-)-0.2		(V+)-0.2	V
Common mode rejection ratio	CMRR	V_{CM} =-0.2V to (V+)+0.2V		57	70	dB
		T_A =-40°C to +125°C		55		dB
INPUT IMPEDENCE				40		
Common mode				1013/2		Ω/pF
differential				1013/4		Ω/pF
OUTPUT	l			1	1	
Voltage output swing from	Voh, Vol	$I_{OUT}=\pm 1$ mA		30	50	mV
rail	1 0117 1 012	1331				
SHUTDOWN						
Shutdown turn-off time	Toff			30		ns
Shutdown turn-on time	Ton			100		ns
SHDN low threshold	V _L	Comparator disabled			(V+)-1.7	V
SHDN high threshold	V _H	Comparator disabled	(V+)-0.9			V
Input bias current of				2		pA
shutdown pin						r
Quiescent current in	I_{QSD}			2		μА
shutdown						Ι'
POWER SUPPLY	200	1		<u> </u>	<u> </u>	
Specified voltage	Vs		2.7		5.5	V
Operating voltage range		Higher end		2.2		V
	_	Lower end		5.5		V
Quiescent current	IQ	V _S =5V, V _O =High		3.2	5	mA
SWITCHING CHARACTERIS		TI. 05%				
	TPD	TA=25°C		5	7	ns
	ΔVIN=100mV, overdrive=20mV	TA=-40°C to +125°C			8	ns
Propagation delay time	TPD	TA=25°C		7.5	10	ns
	ΔVIN=100mV,	TA=-40°C to +125°C			12	ns
	overdrive=5mV	AND 100 N				
Propagation delay skew	ΔT_{SKEW}	ΔVIN=100mV, overdrive=20mV		0.5		ns
Maximum toggle frequency	F _{max}	Overdrive=50mV, V _S =5V		80		MHz
Rise time	T_R			1.5		ns
Fall time	$T_{\rm F}$			1.5		ns



Characteristic plots









Operation description

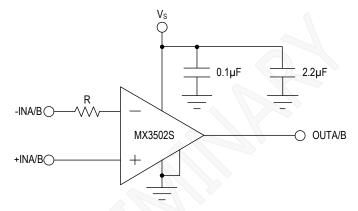
The MX3502S device both feature high speed and include 6mV of internal hysteresis for improved noise immunity with an input common mode range that extends 0.2Vbeyond the power supply rails.

Operating Voltage

The MX3502S comparator is specified for use on a single supply from 1.8V to 5.5V (or a dual supply from ± 1.35 V to ± 2.75 V) over a temperature range of -40°C to +125°C. This device continues to function below this range, but performance is not specified.

Input Over voltage Protection

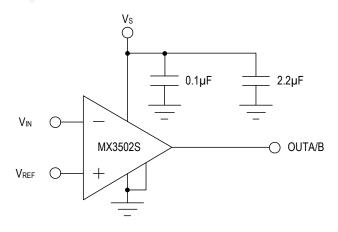
Device inputs are protected by electrostatic discharge diode that conduct if the input voltages exceed the power supplies by more than approximately 300mV. Momentary voltages greater than 300mV beyond the power supply can be tolerated if the input current is limited to 10mA. This limiting is easily accomplished with a small input resistor in series with the comparator, as shown in the below figure.



Input current protection for voltage exceeding the supply voltage

Shutdown

A shutdown pin allows the device to go into idle when it is not in use. When the shutdown pin is high, the device draws approximately 2uA, and the output goes to high impedance. When the shutdown pin is low, the MX3502S is active. When the MX3502S shutdown feature is not used, connect the shutdown pin to the most negative supply, as shown in the below figure. Exiting shutdown mode requires approximately 100ns.



Basic connection for the MX3502S

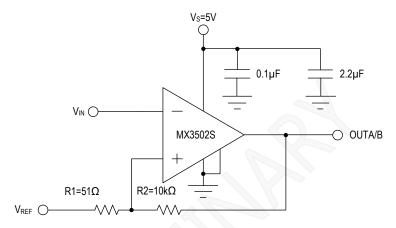
Application Information



The MX3502S has a robust performance when used with a good layout. However, comparator inputs have little noise immunity within the range of a specified offset voltage. For slow moving or noisy input signals, the comparator output can cause an undesirable switch state as input signals move through the switching threshold. In such applications, the 6mV of internal hysteresis of the MX3502S might not be sufficient. For greater noise immunity, external hysteresis can be added by connecting a small amount of feedback to the positive input. The next figure shows a typical topology used to introduce 25mV of additional hysteresis, for a total of 31mV hysteresis when operating from a single 5V supply. Use the following equation to calculate the approximate total hysteresis.

$$V_{HYST} = \frac{(V+) \times R_1}{R_1 + R_2} + 6mV$$

The total hysteresis sets the value of the transition voltage required to switch the comparator output, by enlarging the threshold region, thereby reducing sensitivity to noise.



Power Supply Recommendations

Place bypass capacitors close to the power supply pins to reduce noise coupling in from noisy or high impedance power supplies. For more information on bypass capacitor placement, see Layout Guidelines.

Layout Guidelines

For any high speed comparator or amplifier, proper design and printed circuit board layout are necessary for optimal performance. Excess stray capacitance on the active input, or improper grounding, can limit the maximum performance of high speed circuitry.

Minimizing resistance from source to the comparator input is necessary to minimize the propagation delay of the complete circuit. The source resistance, along with input and stray capacitance, creates an RC filter that delays voltage transitions at the input, and reduces the amplitude of high frequency signals. The input capacitance of the MX3502S, along with stray capacitance from an input pin to ground, results in several picofarads of capacitance.

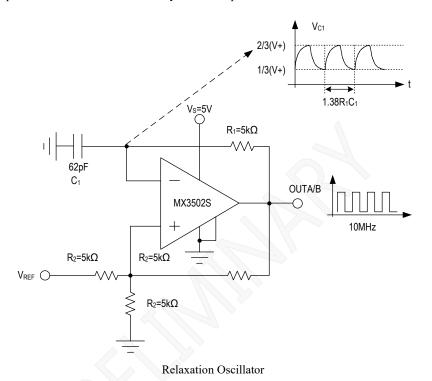
The location and type of capacitance used for power supply bypassing are critical to high speed comparators. The suggested 2.2uF tantalum capacitor does not need to be as close to the device as the 0.1uF capacitor, and may be shared with other devices. The 2.2uF capacitor buffers the power supply line against ripple, and the 0.1uFcapacitor provides a charge for the comparator during high frequency switching.

In a high speed circuit, fast rising and falling switching transients create voltage differences across lines that would be at the same potential at DC. To reduce this effect, use a ground plane to reduce difference in voltage potential within the circuit board. A ground plane has the advantage of minimizing the effect of stray capacitances on the circuit board by proving a more desirable path for the current to flow. With a signal trace over a ground plane, at high frequency the return current (in the ground plane) tends to flow right under the signal trace. Breaks in the ground plane (as simple as through hole leads and vias) in crease the inductance of the plane, making it less effective at higher frequencies. Breaks in the ground plane for necessary vias must be spaces randomly.



Typical application

The MX3502S can easily be configured as a simple and in expensive relaxation oscillator. In the next figure, the R_2 network sets the trip threshold at 1/3 and 2/3 of the supply. Because this circuit is a high speed circuit, the resistor values are low to minimize the effects of parasitic capacitance. The positive input alternates between 1/3 of V+ and 2/3 of V+, depending on whether the output is low or high. The time to charge (or discharge) is $0.69 \times R_1 C_1$. Therefore, the period is $1.38 \times R_1 C_1$. For 62pF and 1kohm as shown in the next figure, the output is calculated to 10.9 MHz. An implementation of this circuit oscillator at 9.6 MHz. Parasitic capacitance and component tolerance explain the difference between theory and actual performance.



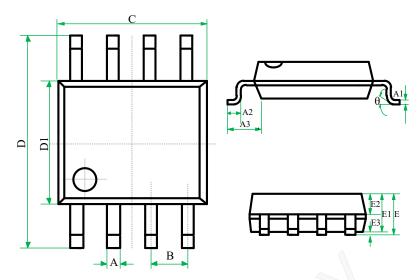
For hysteresis of 1/3 of V+ and threshold levels between 1/3 of V+ and 2/3 of V+, the resistors connected to the comparator positive input must be equal in value. The resistor value must be kept low enough so it does not create additional time constant because of the input capacitor and board parasitic capacitor. The value of the charging resistor R_1 must be relatively low for high frequency switching without drawing high current and affecting the output high and low level. The value of the charging capacitor must be high enough to avoid errors cause by parasitic capacitance.

For the positive input, $IN+=1/3V_{OUT}+1/3V+=1/3V+$, if V_{OUT} is low and assuming V_{OL} is very close to GND. Or, $IN+=1/3V_{OUT}+1/3V+=1/3V+=2/3V+$, if V_{OUT} is high and assuming V_{OH} is very close to V_{OH} .

For the negative input, the capacitor charges to 2/3V+ and discharges to 1/3V+ exponentially at the same rate with a time constant of R_1C_1 .



Package information



SYMBOL	M	MILLIMETERS		INCHES			
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX	
A	0.39	-	0.48	0.0154	-	0.0189	
A1	0.21	-	0.28	0.008	-	0.011	
A2	0.50	-	0.80	0.020	-	0.031	
A3	A3 1.05BSC 0.041BSC			,			
В		1.27BSC			0.050BSC		
С	4.70	4.90	5.10	0.185	0.193	0.201	
D	5.80	6.00	6.20	0.228	0.236	0.244	
D1	3.70	3.90	4.10	0.146	0.154	0.161	
Е		-	1.75	-	-	0.069	
E1	1.30	1.40	1.50	0.051	0.055	0.059	
E2	0.60	0.65	0.70	0.024	0.026	0.028	
E3	0.10	-	0.225	0.004	-	0.009	
θ	0		8°	0	-	8°	

SOP8L for MX3502S



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