GENERAL DESCRIPTION

The MX6875 family of electronic fuses are highly integrated circuit protection and power management solutions in small packages. The device uses very few external components and offers multiple protection modes. They are effective against overloads, short circuits, voltage surges and excessive inrush currents. The MX6875 is a programmable current limit switch with input voltage range selection and output voltage clamping. Extremely low RDS(ON) of the integrated protection N-channel FET helps to reduce power loss during the normal operation.

Applications with special voltage ramp requirements can use a single capacitor to program dVdT to ensure the proper output ramp rate. Independent enable control allows the complicated system sequencing control.

FEATURES

♦Operating input voltage range VIN: 3.3V~14.4V

♦Integrated 28mΩ-on MOS Field Effect Transistor

♦5.9V or 13.6V Fixed Overvoltage Clamp

♦Up to 4A Adjustable Current ILMT

♦Programmable OUT slew rate, undervoltage lockout (UVLO) and overvoltage lockout

♦Built-in thermal shutdown

♦ 10 Pin DFN3*3

APPLICATIONS

♦ Notebook PC

♦ I-pad Mini

♦ Server

♦ Service PC

GENERAL INFORMATION

Ordering information

Part Number	Description
MX6875D33	DFN3*3-10L
MPQ	3000pcs

Package dissipation rating

Package	RθJA(°C/W)
DFN3*3-10L	50

Absolute maximum ratings

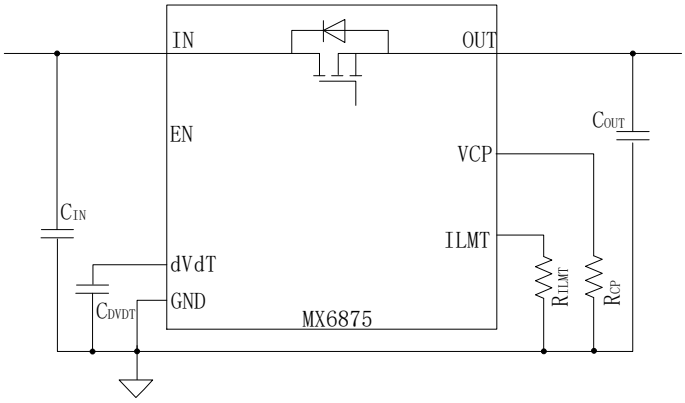
Parameter	Value
VIN	-0.3 to 24V
OUT、VCP	-0.3 to VIN+0.3
I_{OUT}	5A
ILMT、EN、dVdT	-0.3V to 7V
Junction temperature	150°C
Storage temperature, T_{stg}	-55 to 150°C
Leading temperature (soldering, 10secs)	260°C
ESD Susceptibility HBM	±2000V

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

Recommended operating condition

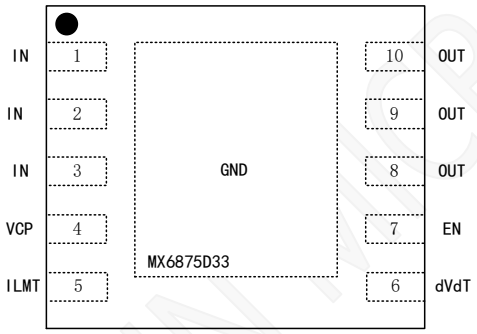
Symbol	Range
VIN、VCP	3.3V to 14.4V
dVdT、EN	0V to 6V
ILMT	0V to 3V
I_{OUT}	0A to 4A
Ambient temperature	-40~85°C
Operating temperature	-40~125°C

TYPICAL APPLICATION



Typical Application

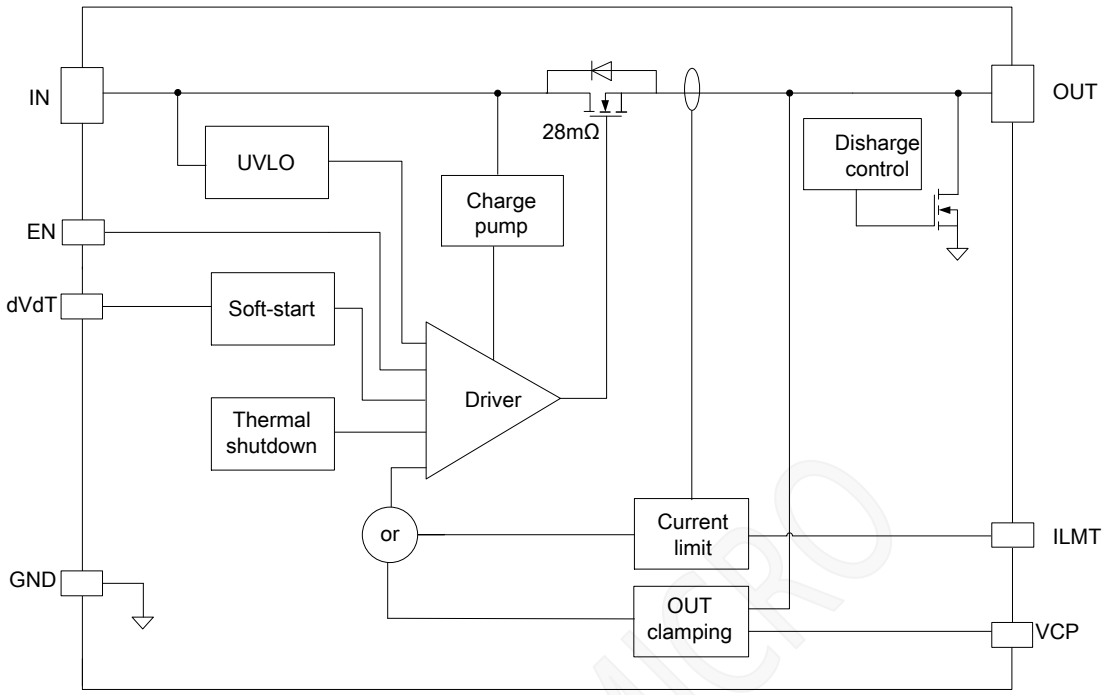
TERMINAL ASSIGNMENTS



Pin information

PIN name	Description	
1、2、3	VIN	Input supply voltage
4	VCP	Output clamp voltage selection based on the input voltage. Pull VCP pin to High by connecting a resistor to IN, or pull VCP pin to Low by connecting a resistor to ground, or float VCP pin to select different output clamping thresholds. Recommend to decoupling this pin with 0.1uF capacitor.
5	ILMT	A resistor from this pin to GND will set the overload and short circuit limit.
6	dVdT	Tie a capacitor from this pin to GND to control the ramp rate of OUT at device turn-on.
7	EN	This is an ENABLE pin. When pulled down, it shuts off the internal pass MOSFET. When pulled high, it enables the device.
8、9、10	OUT	Output of the device
GND	Ground	

BLOCK DIAGRAM



Electrical characteristics

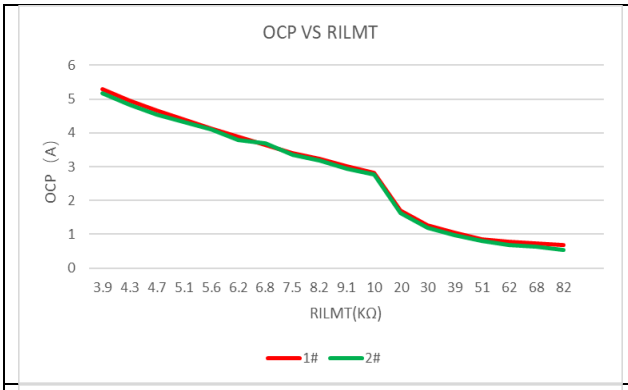
(V_{IN}=12V, V_{EN}=2V, R_{ILMT} = 10kΩ, C_{IN} = C_{OUT} = 100nF, C_{dVdT} = OPEN. T_A = 25°C, unless otherwise noted)

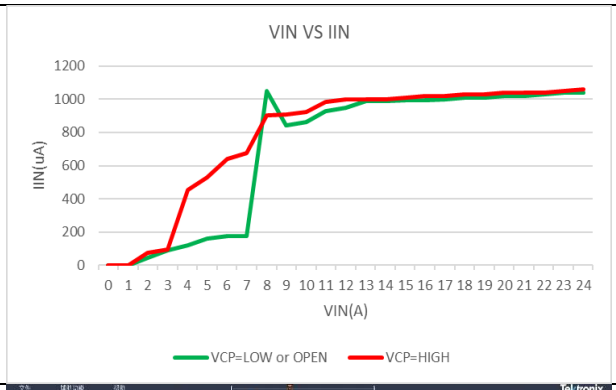
Symbol	Parameter	Test condition	Min	Typ.	Max	Unit
VIN PIN						
V_{UVLO}	UVLO threshold, rising	VCP=High	3.2	3.4	3.6	V
	UVLO threshold, falling		3.1	3.2	3.4	V
	UVLO threshold, rising	VCP=Low or floating	7.8	8.0	8.2(8.5)	V
	UVLO threshold, falling		7.6	7.7	7.8	V
V_{OVC}	Over-voltage clamp	VCP=High, VIN = 8V, I_{OUT} = 10mA	5.4	5.9	6.4	V
		VCP = Low or floating , VIN=15V, I_{OUT} = 10mA	12.8	13.6	14.4	V
I_{IN}	Supply current	Enabled: EN = 2V		0.9		mA
I_Q		EN = 0V		15		uA
EN						
V_{ENR}	EN Threshold voltage, rising		1.20	1.40	1.60	V
V_{ENF}	EN Threshold voltage, falling		1.15	1.35	1.50	V
I_{EN}	EN Input leakage current	0V ≤ V_{EN} ≤ 5V	-100	0.45	100	nA
dVdT						
I_{dVdT}	dVdT charging current		100	200	300	nA
R_{dVdT_disch}	dVdT discharging resistance		50	85	120	Ω
$V_{dVdTmax}$	dVdT max capacitor voltage			5		V
$GAIN_{dVdT}$	dVdT to OUT gain	V_{OUT} : V_{dVdT}		4.85		V/V
t_{dVdT}	Output ramp time	OUT from 0V to 12V, C_{dVdT} = 0		1		ms
		OUT from 0V to 12V, C_{dVdT} = 1nF		10		ms
ILMT						
I_{ILMT}	ILMT leakage current		0.2	0.7	2.2	μA
$V_{OPENILMT}$	ILMT open voltage		2.5	3.7	3.5(	V

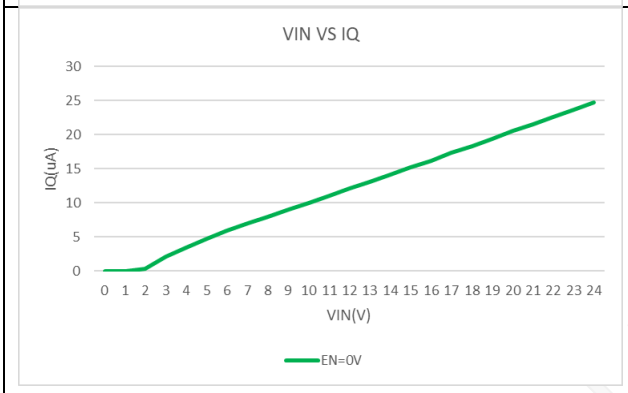
		VILMT Rising, R_{ILMT} = OPEN			4)	
I_{OL}	Overload current limit	R_{ILMT} = 3.9kΩ	4.8	5.2	5.6	A
		R_{ILMT} = 10kΩ	2.5	2.8	3.1	A
		R_{ILMT} = 39kΩ	0.8	1.0	1.2	A
		R_{ILMT} = 68kΩ	0.4	0.6	0.8	A
$I_{OL-R-Short}$	Overload current limit	R_{ILMT} = 0Ω, Shorted Resistor Current Limit		1.6		A
$I_{OL-R-Open}$	Overload current limit	R_{ILMT} = OPEN, Open Resistor Current Limit		1.4		A
I_{SCP}	Short circuit protect current			20		A
$RATIO_{FASTRIP}$	Fast-Trip comparator level : overload current limit	$I_{FASTRIP}$: I_{OL}		160		%
$t_{FastOffDly}$	Fast-Trip comparator delay	I_{OUT} > $I_{FASTRIP}$ to I_{OUT}= 0 (Switch Off)		1		us
OUT						
$R_{DS\ (on)}$	FET ON resistance		20	28	48	mΩ
$I_{OUT-OFF-LKG}$	OUT leakage current in off state	V_{EN} = 0V, V_{OUT} Sourcing	0	4	6	μA
R_{OUT_DISCH}			55	70	110	Ω
TSD						
T_{SHDN}	TSD Threshold, rising			135		℃
$T_{SHDNhyst}$	TSD Hysteresis			-10		℃

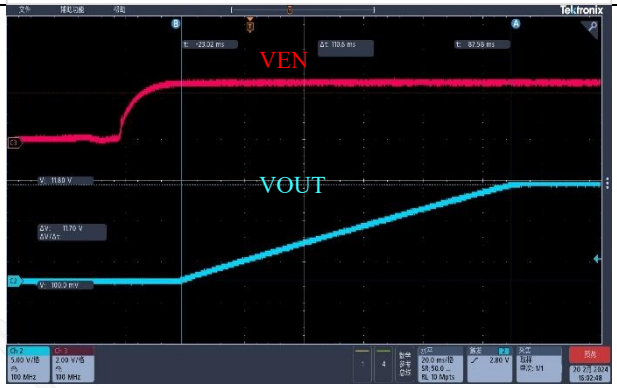
Characteristic plots

VIN = 12V, V_{EN} = 2V, R_{ILMT} = 10kΩ, C_{IN} = C_{OUT} = 1 μF, C_{dvdT} =10nF (unless stated otherwise)



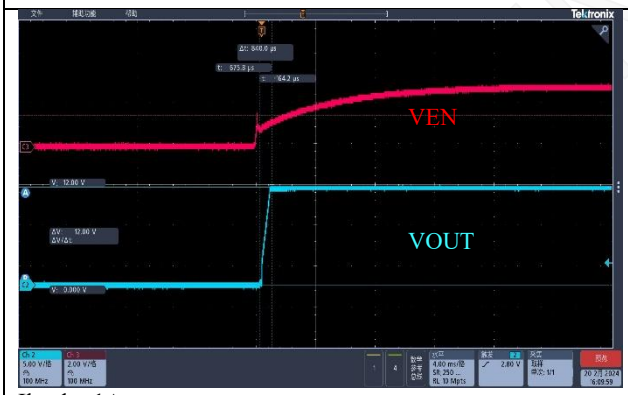






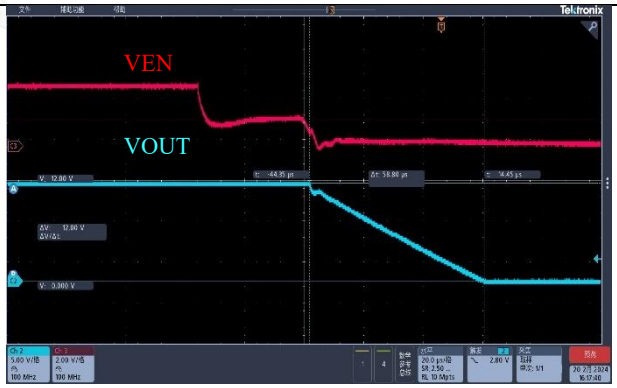
Iload = 1A, CdVdT = 10nF

Soft start



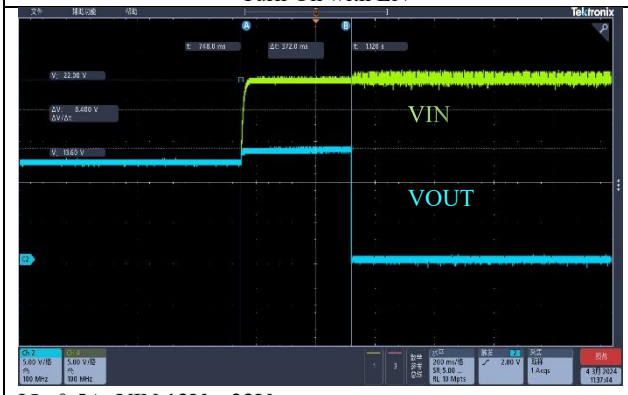
Iload = 1A

Turn On with EN



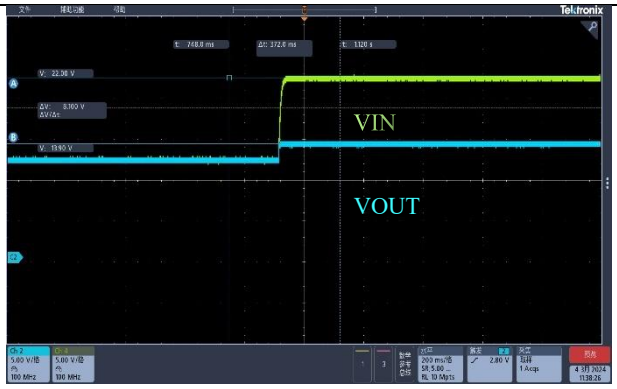
Iload = 1A

Turn Off with EN



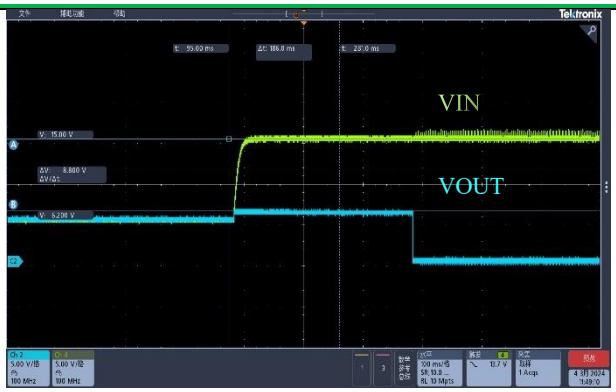
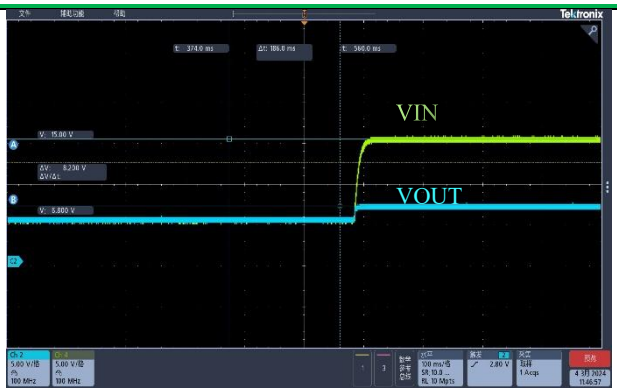
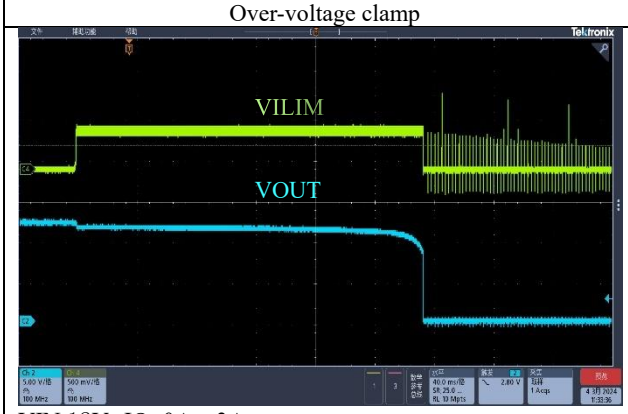
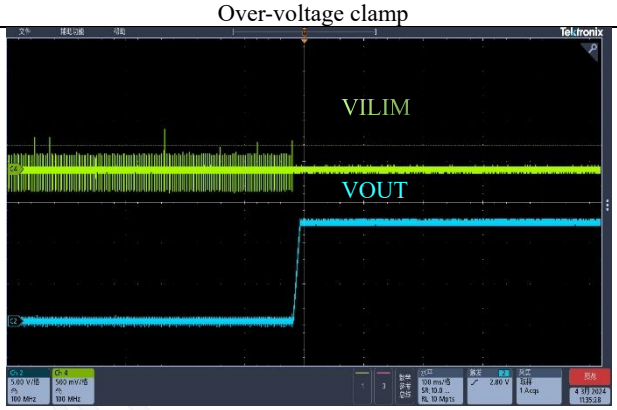
IO=0.5A, VIN:12V→22V

Over-voltage clamp



IO=0A, VIN:12V→22V

Over-voltage clamp

	
IO=0.5A, VCP = HIGH, VIN:5V→15V	IO=0A, VCP = HIGH, VIN:5V→15V
Over-voltage clamp	Over-voltage clamp
	
VIN:12V, IO=0A→3A	VIN:12V, IO=3A→0A
Overload current limit protection	Overload current limit protection released

Operation description

The MX6875 is an e-fuse with integrated power switch that is used to manage current/voltage/start-up voltage ramp to a connected load. The device starts its operation by monitoring the VIN bus. When VIN exceeds the undervoltage-lockout threshold, the device samples the EN pin. A high level on this pin enables the internal MOSFET. As VIN rises, the internal MOSFET of the device will start conducting and allow current to flow from VIN to OUT. When EN is held low (below V_{ENF}), internal MOSFET is turned off.

After a successful start-up sequence, the device now actively monitors its load current and input voltage, ensuring that the adjustable overload current limit I_{OL} is not exceeded, and input voltage spikes are safely clamped to V_{OVC} level at the output. This keeps the output device safe from harmful voltage and current transients. The device also has built-in thermal sensor. In the event device temperature (T_J) exceeds T_{SHDN}, typically 135°C, the thermal shutdown circuitry will shut down the internal MOSFET thereby disconnecting the load from the supply. The MX6875 device will remain off during a cooling period until device temperature falls below T_{SHDN} - 10°C, after which it will attempt to restart. This ON and OFF cycle will continue until fault is cleared.

IN Pin

Input voltage to the MX6875. A ceramic bypass capacitor close to the device from IN to GND is recommended to alleviate bus transients. The recommended operating voltage range is 3.3V to 14V. The device can continuously sustain a voltage of 30V on VIN pin. However, above the recommended maximum bus voltage, MX6875 will be in over-voltage protection (OVP) mode, limiting the output voltage to V_{OVC}. The power dissipation in OVP mode is $P_{D\_OVP} = (V_{IN} - V_{OVC}) \times I_{OUT}$, which can potentially heat up the device and cause thermal shutdown.

dVdT

Connect a capacitor from this pin to GND to control the slew rate of the output voltage at power-on. This pin can be left floating to obtain a predetermined slew rate (minimum T_{dVdT}) on the output. Equation governing slew rate at start-up is shown below:

$$\frac{dV_{OUT}}{dT} = \frac{I_{dVdT} . GAIN_{dVdT}}{C_{dVdT} + C_{INT}}$$

Where:

I_{dVdT} = 200nA (TYP)

C_{INT} = 70pF (TYP)

$GAIN_{dVdT}$ = 4.85

dV_{OUT}/dT = Desired output slew rate

The total ramp time (T_{dVdT}) for 0 to VIN can be calculated using the following equation:

$$T_{dVdT} = 1.03 \times 10^6 \cdot V_{IN} \cdot (C_{dVdT} + 70pF)$$

EN Pin

As an input pin, it controls the ON/OFF state of the internal MOSFET. In its high state, the internal MOSFET is enabled. A low on this pin will turn off the internal MOSFET. High and Low levels are specified in the parametric table of the datasheet. The EN pin is also used to clear a thermal shutdown latch in the MX6875 by toggling this pin high to low.

The internal de-glitch delay on EN falling edge is intentionally kept low (1us typical) for quick detection of power failure. For applications where a higher de-glitch delay on EN is desired, or when the supply is particularly noisy, it is recommended to use an external bypass capacitor from EN to GND.

ILMT Pin

The device continuously monitors the load current and keeps it limited to the value programmed by R_{ILMT}. After start-up event and during normal operation, current limit is set to I_{OL} (over-load current limit).

When power dissipation in the internal MOSFET [$P_D = (V_{IN} - V_{OUT}) \times I_{OUT}$] exceeds 10W, there is a 2% - 12% thermal

foldback in the current limit value so that I_{OL} drops to I_{SC}. In each of the two modes, MOSFET gate voltage is regulated to throttle short-circuit and overload current flowing to the load. Eventually, the device shuts down due to over temperature.

During a transient short circuit event, the current through the device increases very rapidly.

Application and Implementation

Application Information

The MX6875 is a smart eFuse. It is typically used for Hot-Swap and Power rail protection applications. It operates from 3.3V to 14V with programmable current limit and undervoltage protection.

Programming the Current-Limit Threshold: RILMT Selection

The R_{ILMT} resistor at the ILMT pin sets the overload current limit, this can be set using the following table:

RILMT(KΩ)	OCP(A)	RILMT(KΩ)	OCP(A)
3.9	5.29	9.1	3
4.3	4.95	10	2.81
4.7	4.67	20	1.7
5.1	4.4	30	1.27
5.6	4.14	39	1.05
6.2	3.89	51	0.86
6.8	3.65	62	0.77
7.5	3.4	68	0.74
8.2	3.23	82	0.69

Choose closest standard value resistor with 1% tolerance.

Overvoltage Lockout Set Point

Output clamp voltage selection based on the input voltage. Pull VCP pin to High by connecting a resistor to IN, or pull VCP pin to Low by connecting a resistor to ground, or float VCP Pin to select different output clamping thresholds. Recommend to decoupling this pin with 0.1uF capacitor.

VCP	IN		Clamping Threshold		
			min	typ	max
High	5V	Over 6V	5.4V	5.9V	6.4V
Low or floting	12V	Over 14V	12.8V	13.6V	14.4V

Setting Output Voltage Ramp Time T_{dVdT}

For a successful design, the junction temperature of device should be kept below the absolute-maximum rating during both dynamic (start-up) and steady state conditions. Dynamic power stresses often are an order of magnitude greater than the static stresses, so it is important to determine the right start-up time and in-rush current limit required with system capacitance to avoid thermal shutdown during start-up with and without load.

The ramp-up capacitor C_{dVdT} needed is calculated considering the two possible cases:

• Start-up without load: only output capacitance C_{OUT} draws current during start-up

During start-up, as the output capacitor charges, the voltage difference as well as the power dissipated across the internal FET decreases. The average power dissipated in the device during start-up is calculated using the following equation.

For MX6875, the inrush current is determined as:

$$I_{INRUSH} = C_{OUT} \cdot \frac{V_{IN}}{T_{dVdT}}$$

Power dissipation during start-up is:

$$P_{D(INRUSH)} = 0.5 \cdot V_{IN} \cdot I_{INRUSH}$$

The power dissipation equation assumes that load does not draw any current until the output voltage has reached its final value.

• Start-up with load: output capacitance C_{OUT} and load draws current during start-up

When load draws current during the turn-on sequence, there will be additional power dissipated. Considering a resistive load $R_{L(SU)}$ during start-up, load current ramps up proportionally with increase in output voltage during T_{dVdT} time. The average power dissipation in the internal FET during charging time due to resistive load is given by:

$$P_{D(LOAD)} = \frac{V_{IN}^2}{6 \cdot R_{L(SU)}}$$

Total power dissipated in the device during startup is:

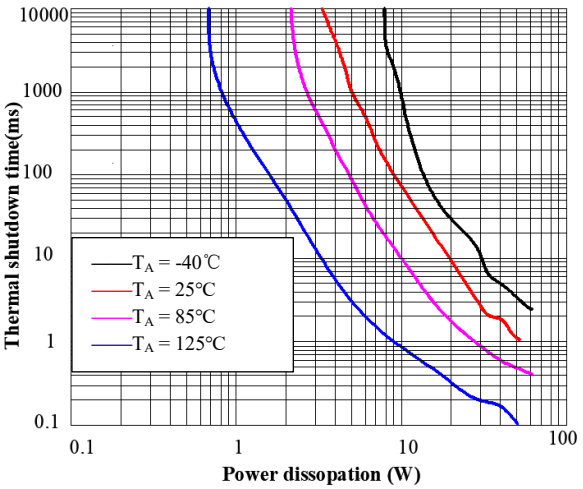
$$P_{D(STARTUP)} = P_{D(INRUSH)} + P_{D(LOAD)}$$

Total current during startup is given by:

$$I_{STARTUP} = I_{INRUSH} + I_L(t)$$

If $I_{STARTUP} > I_{OL}$, the device limits the current to I_{OL} and the current limited charging time is determined by:

$$T_{dVdT(Current-limited)} = C_{OUT} \cdot R_{L(SU)} \cdot \left\{ \frac{I_{OL}}{I_{INRUSH}} - 1 + LN\left[\frac{I_{INRUSH}}{I_{OL} - \frac{V_{IN}}{R_{L(SU)}}} \right] \right\}$$



Support Component Selection - C_{IN}

C_{IN} is a bypass capacitor to help control transient voltages, unit emissions, and local supply noise. Where acceptable, a value in the range of 0.001μF to 0.1μF is recommended for C_{IN}. If the input supply is located more than a few inches from the device an input ceramic bypass capacitor higher than 0.1μF is recommended.

Power Supply Recommendations

Transient Protection

In case of short circuit and overload current limit, when the device interrupts current flow, input inductance generates a positive voltage spike on the input and output inductance generates a negative voltage spike on the output. The peak amplitude of voltage spikes (transients) is dependent on value of inductance in series to the input or output of the device. Such transients can exceed the Absolute Maximum Ratings of the device if steps are not taken to address the issue.

Typical methods for addressing transients include:

• Minimizing lead length and inductance into and out of the device

• Using large PCB GND plane

• Schottky diode across the output to absorb negative spikes

• A low value ceramic capacitor (C_{IN} = 0.001μF to 0.1μF) to absorb the energy and dampen the transients. The approximate value of input capacitance can be estimated with the following equation:

$$V_{SPIKE(Absolute)} = V_{IN} + I_{LOAD} \cdot \sqrt{\frac{L_{IN}}{C_{IN}}}$$

Where:

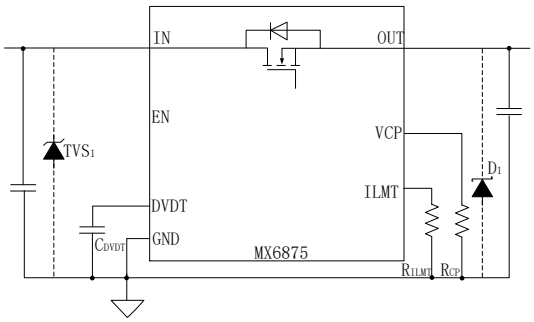
• V_{IN} is the nominal supply voltage

• I_{LOAD} is the load current

• L_{IN} equals the effective inductance seen looking into the source

• C_{IN} is the capacitance present at the input

Some applications may require the addition of a Transient Voltage Suppressor (TVS) to prevent transients from exceeding the Absolute Maximum Ratings of the device.



Output Short-Circuit Measurements

It is difficult to obtain repeatable and similar short-circuit testing results. Source bypassing, input leads, circuit layout and component selection, output shorting method, relative location of the short, and instrumentation all contribute to

variation in results. The actual short itself exhibits a certain degree of randomness as it microscopically bounces and arcs. Care in configuration and methods must be used to obtain realistic results. Do not expect to see waveforms exactly like those in the datasheet.

Layout Guidelines

For all applications, a 0.01μF or greater ceramic decoupling capacitor is recommended between IN terminal and GND. For hot-plug applications, where input power path inductance is negligible, this capacitor can be eliminated or minimized.

• The optimum placement of decoupling capacitor is closest to the IN and GND terminals of the device. Care must be taken to minimize the loop area formed by the bypass-capacitor connection, the IN terminal, and the GND terminal of MX6875.

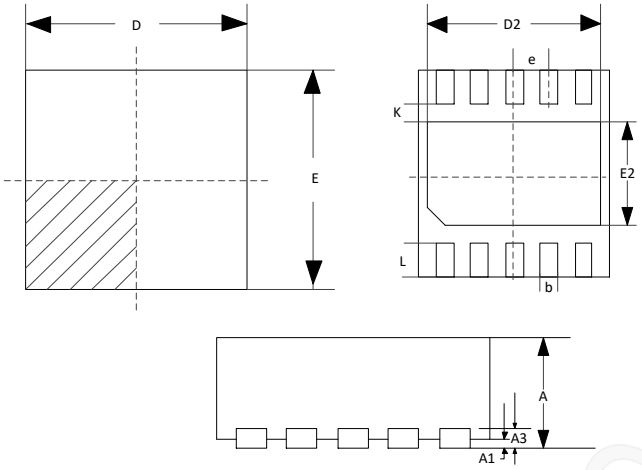
• High current carrying power path connections should be as short as possible and should be sized to carry at least twice the full-load current.

• The GND terminal must be tied to the PCB ground plane at the terminal of MX6875. The PCB ground should be a copper plane or island on the board.

• Locate all support components: R_{ILMT}, C_{dVdT} and resistors for EN, close to their connection pin. Connect the other end of the component to the GND pin of the device with shortest trace length. The trace routing for the R_{ILMT} and C_{dVdT} components to the device should be as short as possible to reduce parasitic effects on the current limit and soft start timing. These traces should not have any coupling to switching signals on the board.

• Protection devices such as TVS, snubbers, capacitors, or diodes should be placed physically close to the device they are intended to protect and routed with short traces to reduce inductance. For example, a protection Schottky diode is recommended to address negative transients due to switching of inductive loads, and it should be physically close to the OUT pins.

Package information DFN3*3-10L



SYMBOL	MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.03	0.05
A3		0.20REF	
b	0.18	0.24	0.30
D		3.00BSC	
D2	2.45	2.50	2.55
E		3.00BSC	
E2	1.75	1.80	1.85
e		0.50BSC	
K		0.19TYP	
L	0.35	0.40	0.45

DFN3*3-10L for MX6875D33

Restrictions on Product Use

◆ MAXIN micro is continually working to improve the quality and reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing MAXIN products, to comply with the standards of safety in making a safe design for the entire system, and to avoid situations in which a malfunction or failure of such MAXIN products could cause loss of human life, bodily injury or damage to property.

◆ In developing your designs, please ensure that MAXIN products are used within specified operating ranges as set forth in the most recent MAXIN products specifications.

◆ The information contained herein is subject to change without notice.

Version update record:

V10 The original version (preliminary)

V11 Updated Package information of DFN3*3-10L

V12 Updated Package information of DFN3*3-10L