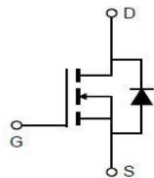
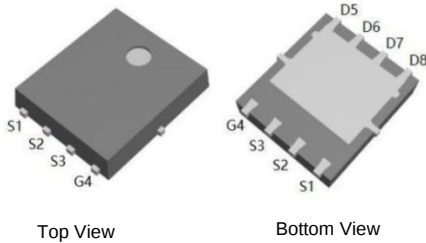


Product Summary

V_{DS}	$R_{DS(ON_MAX)}$	I_{D_MAX}
40 V	1.8 m Ω @ $V_{GS} = 10V$	140 A

DFN5*6



Schematic Diagram

Features

- Uses advanced Perfect MOS5 technology
- Excellent FoM (figure of merit)
- Extremely low on-resistance $R_{DS(on)}$
- 100% UIS dVds and R_g tested
- Qualified according to JEDEC criteria



Applications

- DC/DC in Telecoms and Industrial
- Synchronous Rectification in SMPS
- Li-battery protection

Benefits

- High robustness and reliability
- Increases maximum current capability
- Low power loss, high power density
- Easy paralleling

Ordering Information

Orderable Part Number	Package Type	Device Marking	Form	Quantity (pcs)
MX4001D56	DFN5*6	4001D56	13" Tape&Reel	5,000

Maximum Ratings (@ $T_C = 25^\circ\text{C}$, unless otherwise specified.)

Parameter	Symbol	Value	Unit
Drain - Source Voltage	V_{DS}	40	V
Gate - Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ($V_{GS} = 10V$) ⁽¹⁾	I_D	140	A
		78	A
Pulsed Drain Current ⁽²⁾	I_{DM}	560	A
Single Pulse Avalanche Energy ⁽³⁾	E_{AS}	196	mJ
Power Dissipation	P_D	95	W
Junction & Storage Temperature Range	T_J, T_{STG}	-55 ~ +150	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Typ.	Max.	Unit
Thermal Resistance, Junction-to-Ambient ⁽⁴⁾	$R_{\theta JA}$		50	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Case ⁽⁵⁾	$R_{\theta JC}$		1.5	$^\circ\text{C/W}$

Electrical Characteristics (@ $T_J = 25^\circ\text{C}$, unless otherwise specified.)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Off Characteristics ⁽⁶⁾						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250μA	40	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 40V, V _{GS} = 0V T _J = 125°C	-	-	1.0	μA
			-	-	100	μA
Gate-Source Leakage Current	I _{GSS}	V _{GS} = ±20V, V _{DS} = 0V	-	-	±100	nA
On Characteristics ⁽⁶⁾						
Gate Threshold Voltage	V _{GS(th)}	V _{GS} = V _{DS} , I _D = 250μA	2.0	-	3.5	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} = 10V, I _D = 20A	-	1.55	2.0	mΩ
Forward Transconductance	g _{fs}	V _{DS} = 5.0V, I _D = 20A	-	43	-	S
Diodes Forward Voltage	V _{SD}	I _S = 20.0A, V _{GS} = 0V	-	0.7	1.2	V
Dynamic Characteristics ⁽⁷⁾						
Input Capacitance	C _{iss}	V _{DS} = 20V, V _{GS} = 0V, f = 1MHz	-	3699	-	pF
Output Capacitance	C _{oss}		-	1880	-	pF
Reverse Transfer Capacitance	C _{rss}		-	105	-	pF
Gate Resistance	R _g	V _{GS} = 0V, V _{DS} = 0V, f = 1MHz	-	2.2	-	Ω
Switching Characteristics ⁽⁷⁾						
Turn-On DelayTime	t _{d(on)}	V _{GS} = 10V, V _{DS} = 20V I _D = 30A, R _{GEN} = 2.2Ω	-	17	-	ns
Rise Time	t _r		-	18.2	-	ns
Turn-Off DelayTime	t _{d(off)}		-	45	-	ns
Fall Time	t _f		-	11.6	-	ns
Gate Charge Characteristics ⁽⁷⁾						
Total Gate Charge (V _{GS} = 10V)	Q _g	V _{DS} = 20V, I _D = 50A V _{GS} = 10V	-	62	-	nC
Gate-Source Charge	Q _{gs}		-	20	-	nC
Gate-Drain Charge	Q _{gd}		-	9	-	nC
Drain-Source Diode Characteristics ⁽⁷⁾						
Body Diode Reverse Recovery Time	t _{rr}	I _F = 35A, Vr=30V,dI/dt = 100A/μs, T _J = 25°C	-	98	-	ns
Body Diode Reverse Recovery Charge	Q _{rr}		-	199	-	nC
Diode Forward Current	I _S	T _C = 25°C	-	-	140	A

Notes:

1. This current is chip limited, which is calculated based on R_{thjc} .
2. This current is calculated on single pulse with $10\mu s$ Pulse & Duty Cycle = 1%.
3. Device mounted on FR-4 substrate PC board with 2oz copper in 1inch square cooling area.
4. Thermal resistance from junction to soldering point (on the exposed drain pad).
5. Short duration pulse test used to minimize self-heating effect.
6. Defined by design, not subject to production.

Typical Performance Characteristics

Fig 1: Output Characteristics

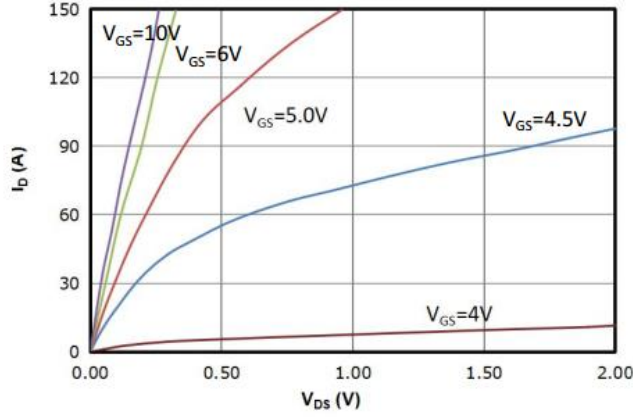


Fig 2: Transfer Characteristics

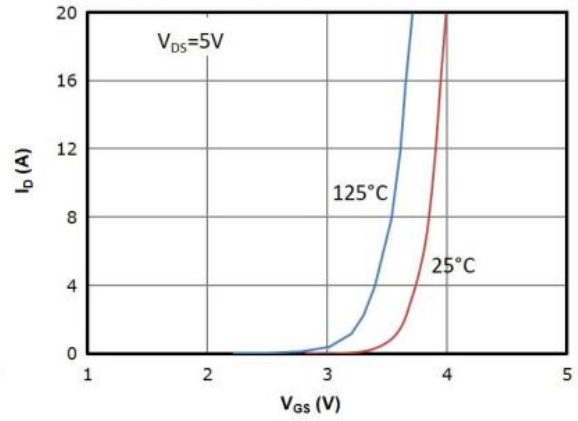


Fig 3: $R_{DS(on)}$ vs Drain Current and Gate Voltage

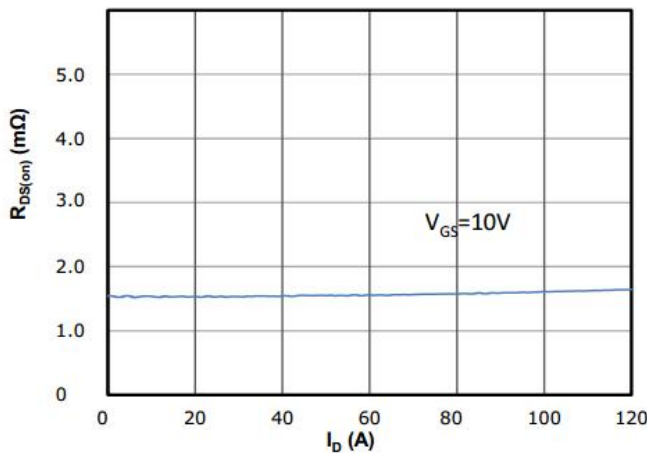


Fig 4: $R_{DS(on)}$ vs Gate Voltage

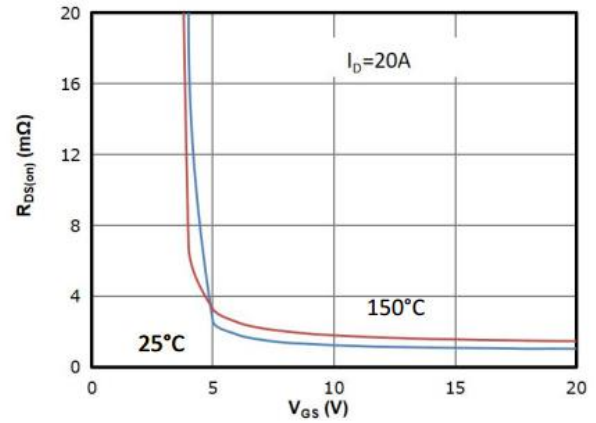


Fig 5: $R_{DS(on)}$ vs. Temperature

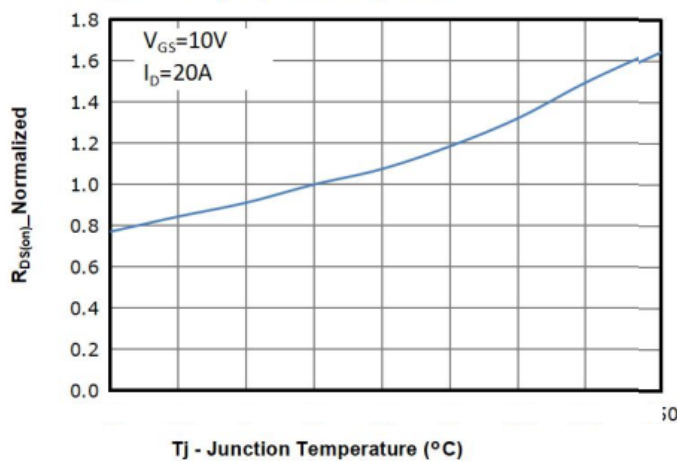


Fig 6: $V_{GS(th)}$ vs. Temperature

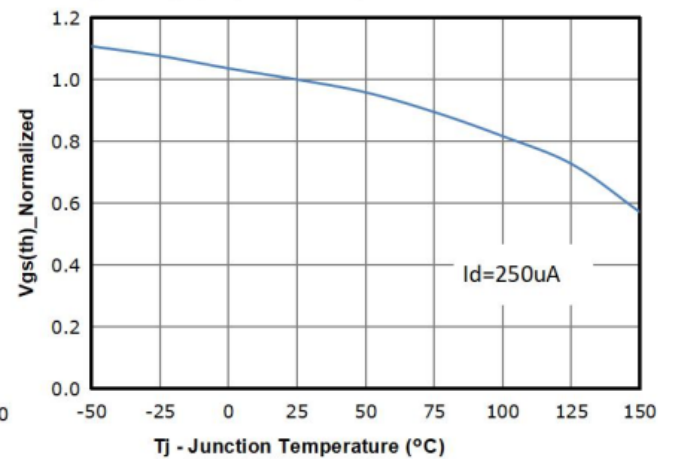


Fig 7: BVdss vs. Temperature

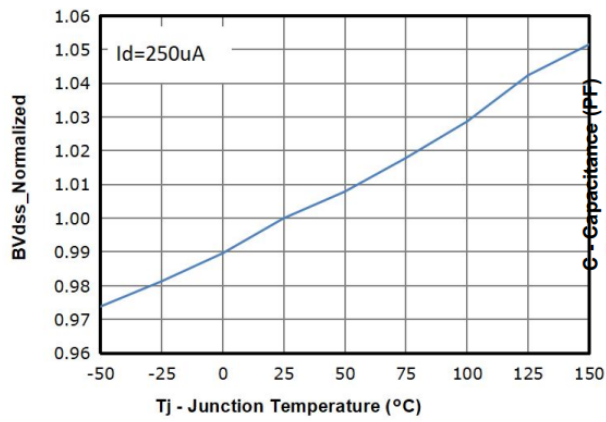


Fig 8: Capacitance Characteristics

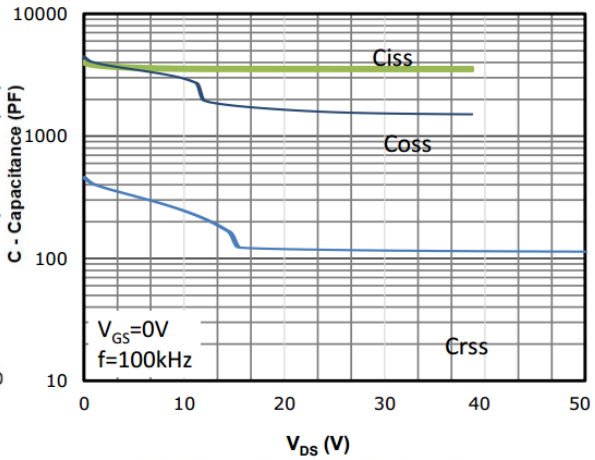


Fig 9: Gate Charge Characteristics

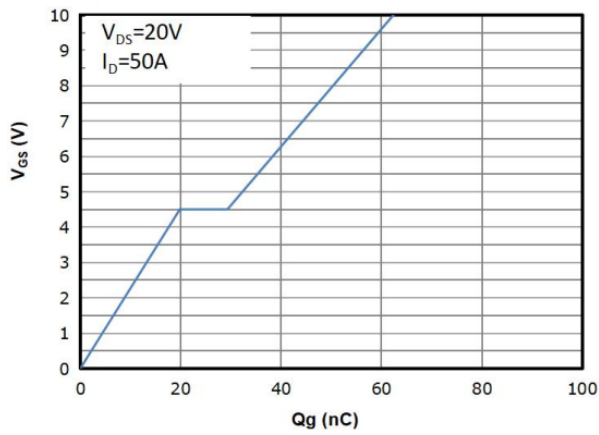


Fig 10: Body-diode Forward Characteristics

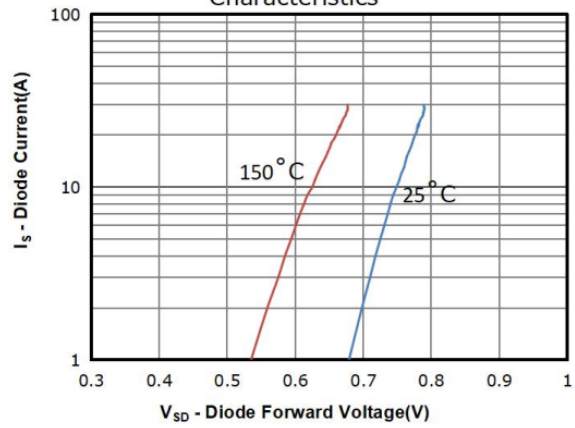


Fig 11 :Power Dissipation

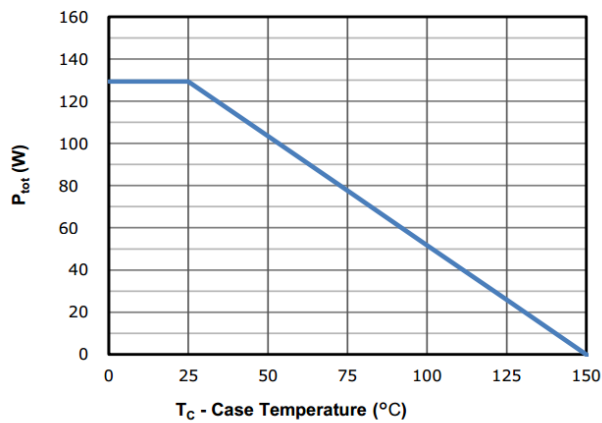


Fig12: Drain Current Derting

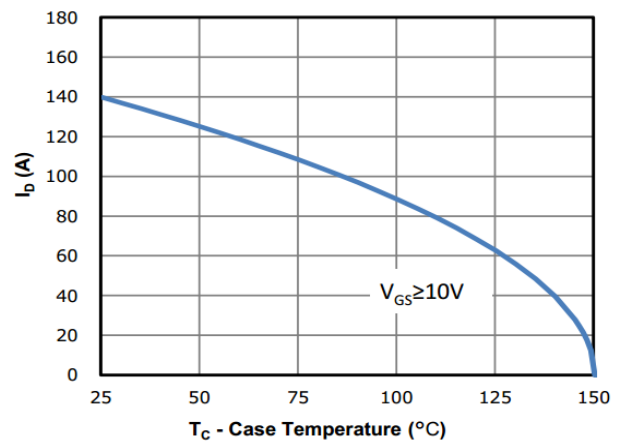


Fig 13: Safe Operating Area

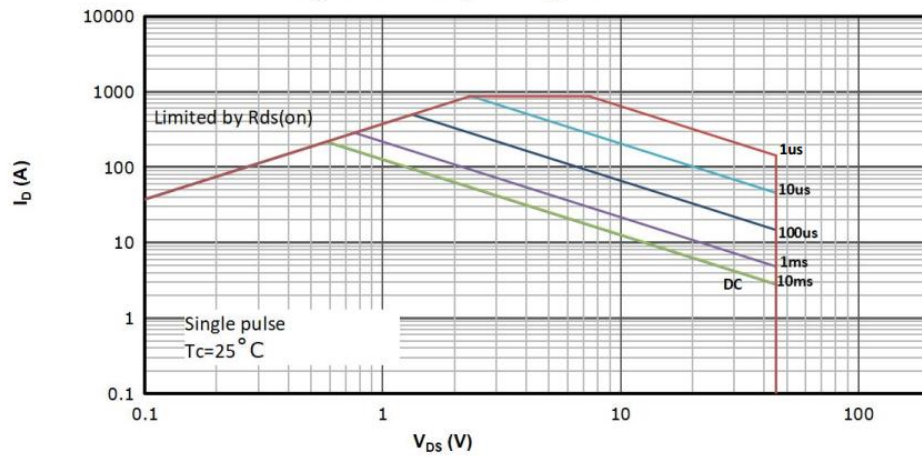
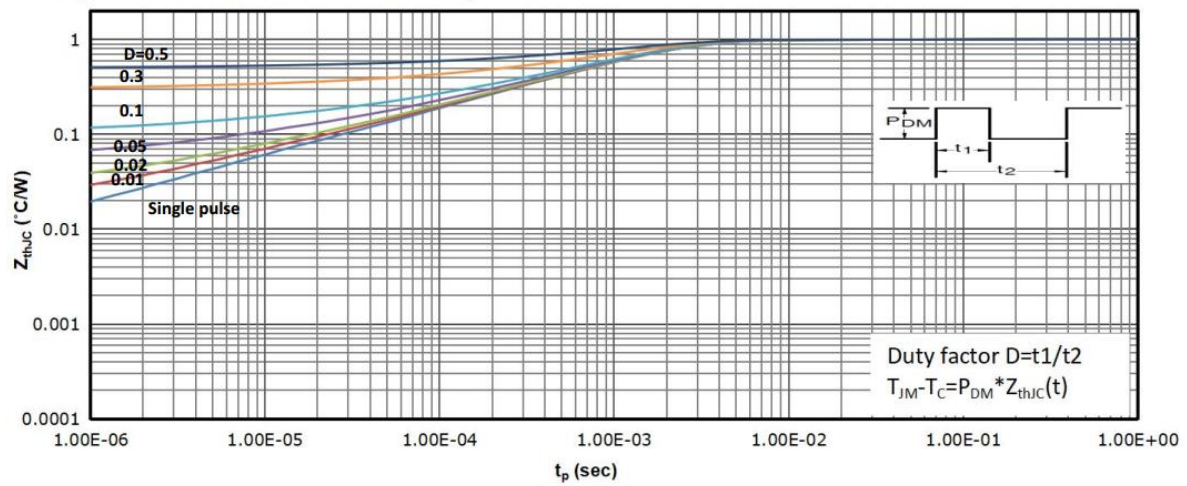


Fig 14: Max. Transient Thermal Impedance



Test Circuit and Waveform

Figure A: Gate Charge Test Circuit and Waveform

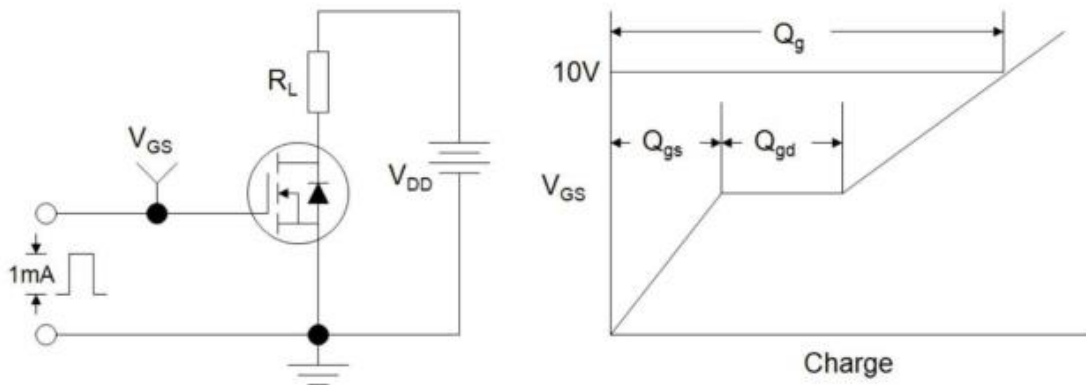


Figure B: Resistive Switching Test Circuit and Waveform

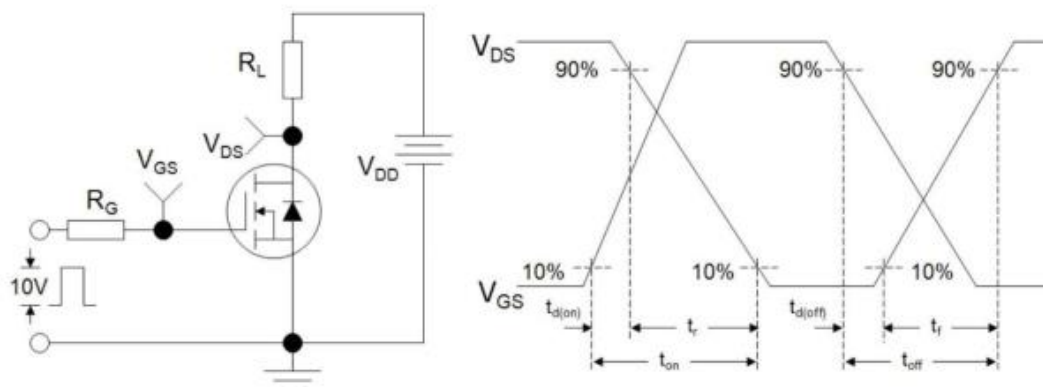
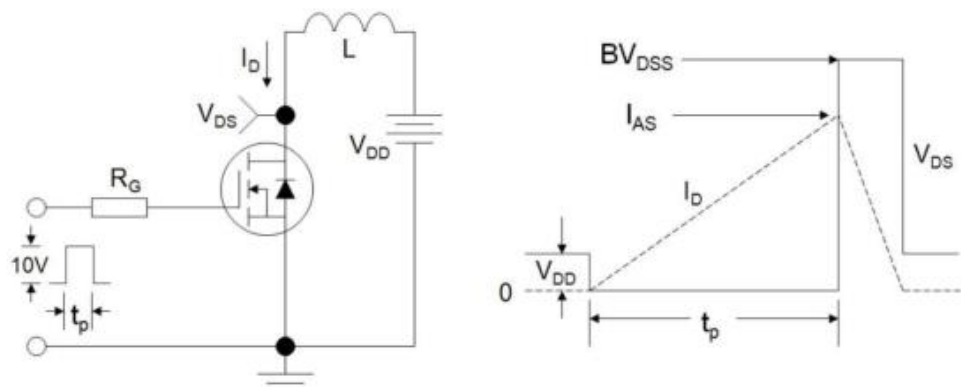
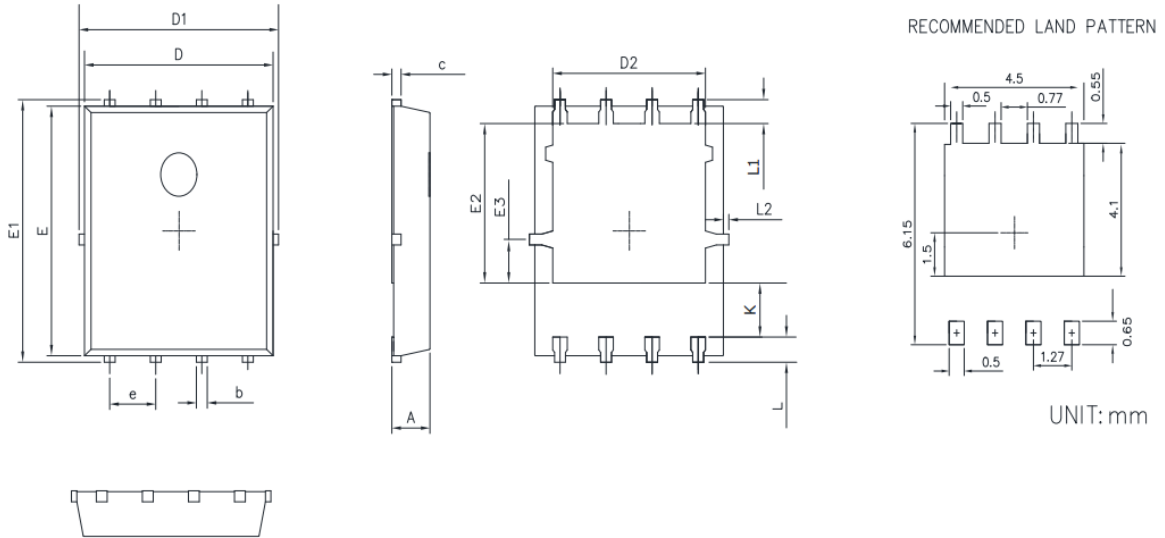


Figure C: Unclamped Inductive Switching Test Circuit and Waveform



Package Outline: DFN5X6



SYMBOL	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.90	1.10	0.035	0.043
b	0.25	0.50	0.010	0.020
c	0.10	0.30	0.004	0.012
D	4.80	5.30	0.189	0.209
D1	4.90	5.50	0.193	0.217
D2	3.92	4.20	0.154	0.165
E	5.65	5.85	0.222	0.230
E1	5.90	6.20	0.232	0.244
E2	3.33	3.78	0.131	0.149
E3	0.80	1.00	0.031	0.039
e	1.27		0.050	
L	0.40	0.70	0.016	0.028
L1	0.65		0.026	
L2	0.00	0.15	0.000	0.006
K	1.00	1.50	0.039	0.059