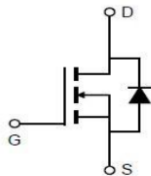
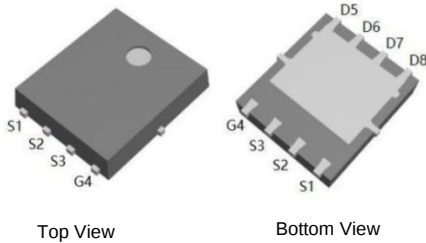


Product Summary

V_{DS}	$R_{DS(ON)}_{typ}$	I_{D_MAX}
30 V	2.5 m Ω @ $V_{GS} = 10V$	122 A

DFN5*6



Schematic Diagram

Features

- Uses advanced trench technology
- Excellent FoM (figure of merit)
- Extremely low on-resistance $R_{DS(on)}$
- 100% UIS dVds and R_g tested
- Qualified according to JEDEC criteria



Applications

- DC/DC in Telecoms and Industrial
- Synchronous Rectification in SMPS
- Li-battery protection

Benefits

- High robustness and reliability
- Increases maximum current capability
- Low power loss, high power density
- Easy paralleling

Ordering Information

Orderable Part Number	Package Type	Device Marking	Form	Quantity (pcs)
MX3003D56	DFN5*6	3003D56	13" Tape&Reel	5,000

Maximum Ratings (@ $T_C = 25^\circ\text{C}$, unless otherwise specified.)

Parameter	Symbol	Value	Unit
Drain - Source Voltage	V_{DS}	30	V
Gate - Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ($V_{GS} = 10V$) ⁽¹⁾	$T_C = 25^\circ\text{C}$	122	A
	$T_C = 100^\circ\text{C}$	77	A
Pulsed Drain Current ⁽²⁾	I_{DM}	488	A
Single Pulse Avalanche Energy ⁽³⁾	E_{AS}	289	mJ
Power Dissipation	$T_C = 25^\circ\text{C}$	76	W
	$T_C = 100^\circ\text{C}$	25	W
Junction & Storage Temperature Range	T_J, T_{STG}	-55 ~ +150	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Typ.	Max.	Unit
Thermal Resistance, Junction-to-Ambient ⁽⁴⁾	$R_{\theta JA}$		62	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Case ⁽⁵⁾	$R_{\theta JC}$		1.5	$^\circ\text{C/W}$

Electrical Characteristics (@ $T_J = 25^\circ\text{C}$, unless otherwise specified.)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Off Characteristics ⁽⁶⁾						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250μA	30	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 30V, V _{GS} = 0V T _J = 125°C	-	-	1.0	μA
			-	-	100	μA
Gate-Source Leakage Current	I _{GSS}	V _{GS} = ±20V, V _{DS} = 0V	-	-	±100	nA
On Characteristics ⁽⁶⁾						
Gate Threshold Voltage	V _{GS(th)}	V _{GS} = V _{DS} , I _D = 250μA	1.0	-	2.5	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} = 10V, I _D = 20A	-	2.5	3.2	mΩ
Forward Transconductance	g _{fs}	V _{DS} = 5.0V, I _D = 20A	-	40	-	S
Diodes Forward Voltage	V _{SD}	I _S = 20.0A, V _{GS} = 0V	-	0.7	1.2	V
Dynamic Characteristics ⁽⁷⁾						
Input Capacitance	C _{iSS}	V _{DS} = 15V, V _{GS} = 0V, f = 1MHz	-	3280	-	pF
Output Capacitance	C _{oSS}		-	344	-	pF
Reverse Transfer Capacitance	C _{rSS}		-	302	-	pF
Gate Resistance	R _g	V _{GS} = 0V, V _{DS} = 0V, f = 1MHz	-	2.0	-	Ω
Switching Characteristics ⁽⁷⁾						
Turn-On DelayTime	t _{d(on)}	V _{GS} = 10V, V _{DS} = 15V I _D = 20A, R _{GEN} = 3.0Ω	-	25	-	ns
Rise Time	t _r		-	21	-	ns
Turn-Off DelayTime	t _{d(off)}		-	50	-	ns
Fall Time	t _f		-	27	-	ns
Gate Charge Characteristics ⁽⁷⁾						
Total Gate Charge (V _{GS} = 10V)	Q _g	V _{DS} = 15V, I _D = 20A V _{GS} = 10V	-	56	-	nC
Gate-Source Charge	Q _{gs}		-	7.5	-	nC
Gate-Drain Charge	Q _{gd}		-	16	-	nC
Drain-Source Diode Characteristics ⁽⁷⁾						
Body Diode Reverse Recovery Time	t _{rr}	I _F = 20A, dI/dt = 100A/μs,	-	56	-	ns
Body Diode Reverse Recovery Charge	Q _{rr}	T _J = 25°C	-	42	-	nC
Diode Forward Current	I _S	T _C = 25°C	-	-	122	A

Notes:

1. This current is chip limited, which is calculated based on R_{thjc} .
2. This current is calculated on single pulse with $10\mu s$ Pulse & Duty Cycle = 1%.
3. Device mounted on FR-4 substrate PC board with 2oz copper in 1inch square cooling area.
4. Thermal resistance from junction to soldering point (on the exposed drain pad).
5. Short duration pulse test used to minimize self-heating effect.
6. Defined by design, not subject to production.

Typical Characteristics

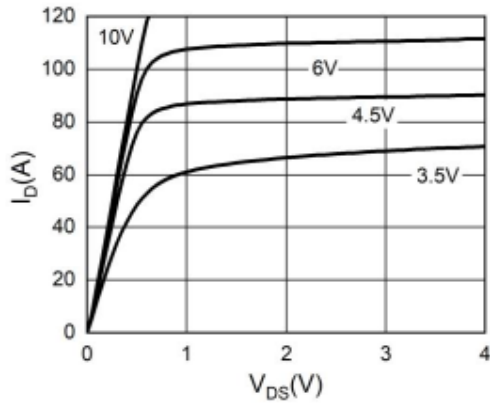


Figure 1. Output Characteristics

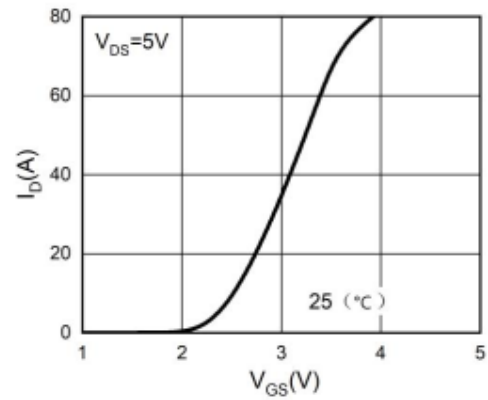


Figure 2. Transfer Characteristics

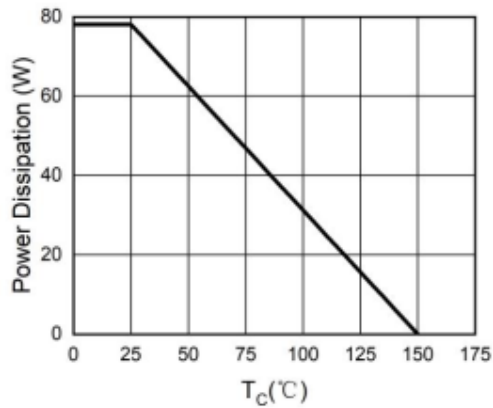


Figure 3. Power Dissipation

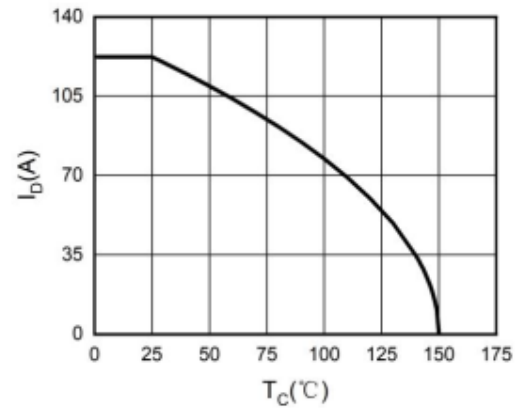


Figure 4. Drain Current

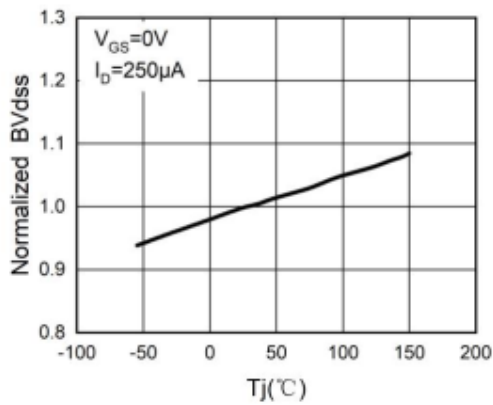


Figure 5. BV_DS vs Junction Temperature

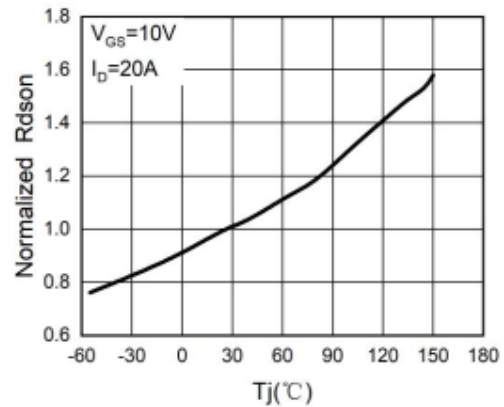


Figure 6. R_DS(on) vs Junction Temperature

Typical Characteristics

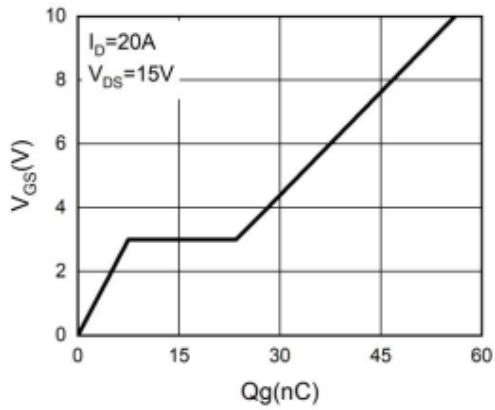


Figure 7. Gate Charge Waveforms

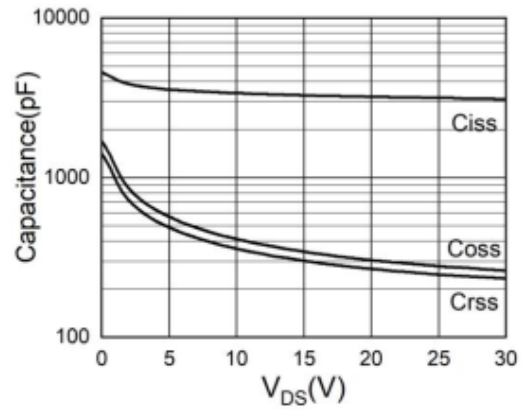


Figure 8. Capacitance

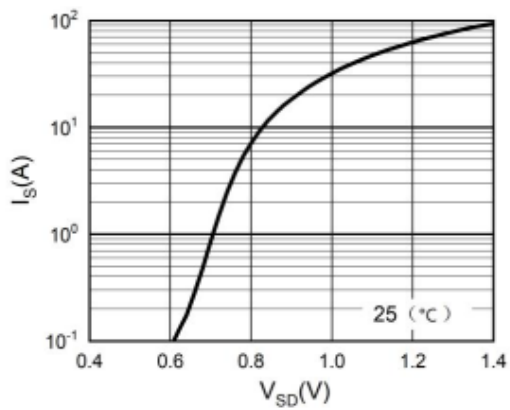


Figure 9. Body-Diode Characteristics

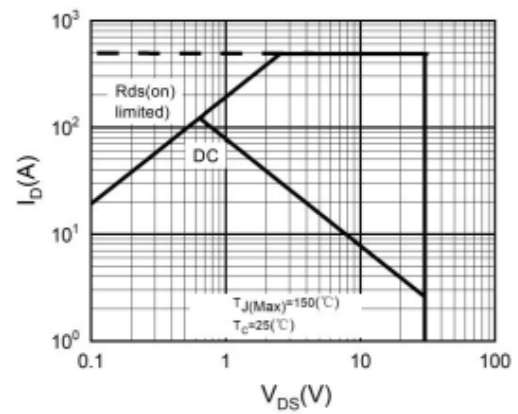


Figure 10. Maximum Safe Operating Area

Test Circuit and Waveform

Figure A: Gate Charge Test Circuit and Waveform

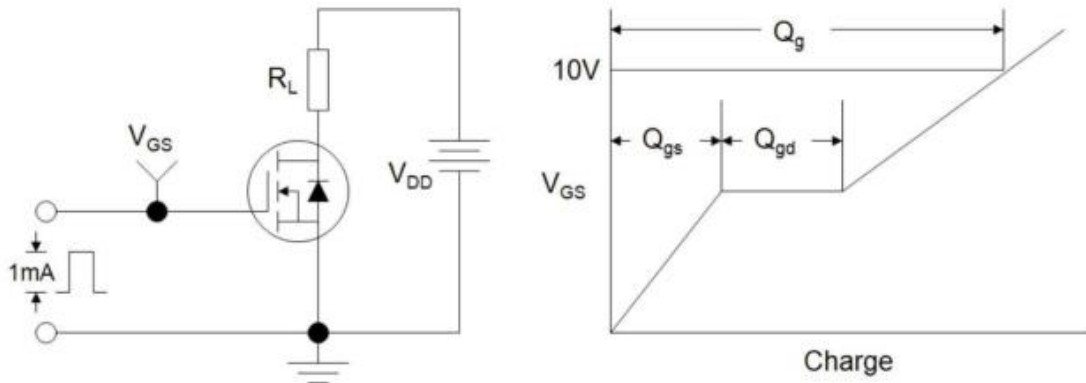


Figure B: Resistive Switching Test Circuit and Waveform

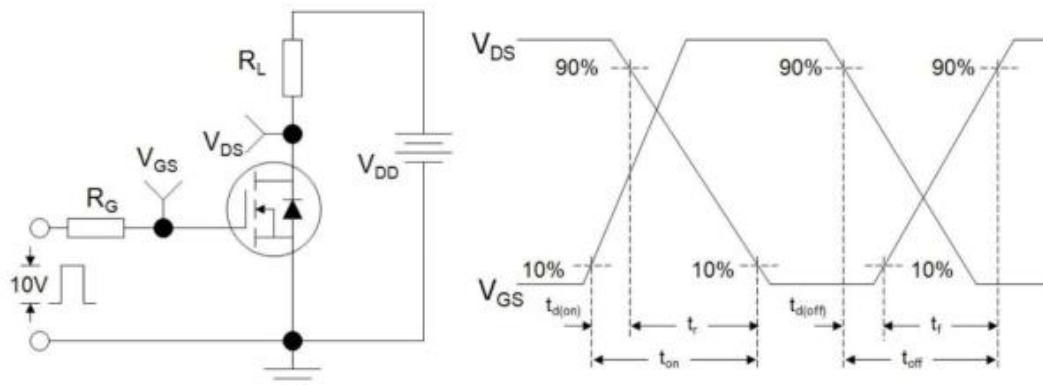
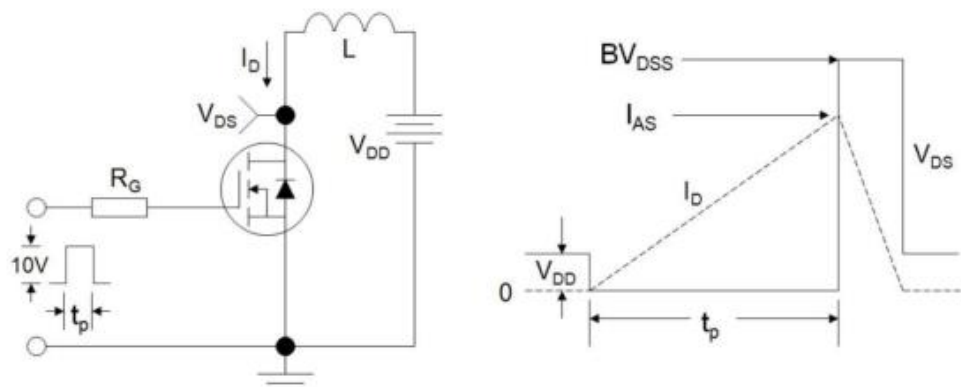
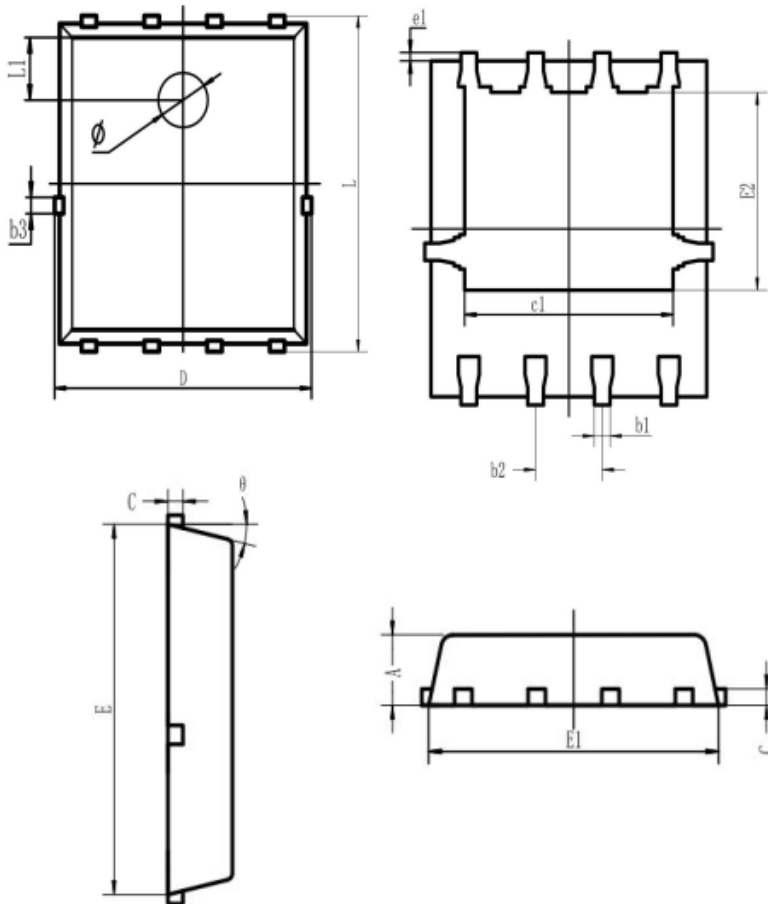


Figure C: Unclamped Inductive Switching Test Circuit and Waveform



Package Information (PDFN5×6-8 PACKAGE)



COMMON DIMENSIONS (UNITS OF MEASURE IS mm)			
SYMBOLS	MIN	NORMAL	MAX
A	0.95	1.00	1.17
b1	0.25	0.30	0.35
b2	1.22	1.27	1.32
b3	0.20	0.25	0.30
C	0.20	0.25	0.30
c1	3.90	4.00	4.10
D	4.80	5.00	5.40
E	5.70	5.75	5.90
E1	4.80	4.90	5.00
E2	3.38	3.48	3.58
e1	0.095	0.125	0.200
L	5.95	6.00	6.35
L1	1.30	1.40	1.50
θ	0°	10°	13°
ϕ	0.90	1.00	1.10