无锡明芯微
MAXINMICRO

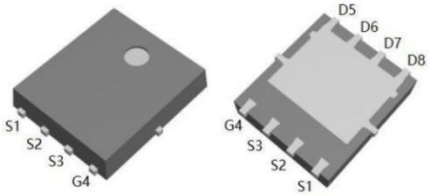
MX4003D56

40V N-Channel Power MOSFET

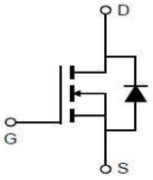
Product Summary

V_{DS}	$R_{DS(ON)\_MAX}$	I_{D_MAX}
40 V	3 mΩ @V_{GS} = 10V	108 A

DFN5*6



Top View Bottom View



Schematic Diagram

Features

- Uses advanced Perfect MOS5 technology
- Excellent FoM (figure of merit)
- Extremely low on-resistance RDS(on)
- 100% UIS dVds and R_g tested
- Qualified according to JEDEC criteria

RoHS HALOGEN FREE

Applications

- DC/DC in Telecoms and Inductrial
- Synchronous Rectification in SMPS
- Li-battery protection

Benefits

- High robustness and reliability
- Increases maximum current capability
- Low power loss, high power density
- Easy paralleling

Ordering Information

Orderable Part Number	Package Type	Device Marking	Form	Quantity (pcs)
MX4003D56	DFN5*6	4003D56	13" Tape&Reel	5,000

Maximum Ratings (@ T_C = 25°C, unless otherwise specified.)

Parameter		Symbol	Value	Unit
Drain - Source Voltage		V_{DS}	40	V
Gate - Source Voltage		V_{GS}	±20	V
Continuous Drain Current (V_{GS} = 10V) (1)	T_C = 25°C	I_D	108	A
	T_C = 100°C		68	A
Pulsed Drain Current (2)		I_{DM}	432	A
Single Pulse Avalanche Energy (3)		E_{AS}	185	mJ
Power Dissipation	T_C = 25°C	P_D	78	W
Junction & Storage Temperature Range		T_J, T_{STG}	-55 ~ +150	°C

Thermal Characteristics

Parameter	Symbol	Typ.	Max.	Unit
Thermal Resistance, Junction-to-Ambient (4)	$R_{\theta JA}$		50	°C/W
Thermal Resistance, Junction-to-Case (5)	$R_{\theta JC}$		1.6	°C/W

Electrical Characteristics (@ T_J = 25°C, unless otherwise specified.)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Off Characteristics [6]						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	42	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40V, V_{GS} = 0V	-	-	1.0	μA
		T_J = 125°C	-	-	100	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20V, V_{DS} = 0V	-	-	±100	nA
On Characteristics [6]						
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 250μA	2.0	-	3.5	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS} = 10V, I_D = 20A	-	2.65	3	mΩ
Forward Transconductance	g_{fs}	V_{DS} = 5.0V, I_D = 20A	-	43	-	S
Diodes Forward Voltage	V_{SD}	I_S = 20.0A, V_{GS} = 0V	-	0.8	1.2	V
Dynamic Characteristics [7]						
Input Capacitance	C_{iss}	V_{DS} = 20V, V_{GS} = 0V, f = 1MHz	-	2200	-	pF
Output Capacitance	C_{oss}		-	1420	-	pF
Reverse Transfer Capacitance	C_{rss}		-	55	-	pF
Gate Resistance	R_g	V_{GS} = 0V, V_{DS} = 0V, f = 1MHz	-	2	-	Ω
Switching Characteristics [7]						
Turn-On DelayTime	$t_{d(on)}$	V_{GS} = 10V, V_{DS} = 20V I_D = 30A, R_{GEN} = 2.2Ω	-	13	-	ns
Rise Time	t_r		-	33	-	ns
Turn-Off DelayTime	$t_{d(off)}$		-	45	-	ns
Fall Time	t_f		-	23	-	ns
Gate Charge Characteristics [7]						
Total Gate Charge (V_{GS} = 10V)	Q_g	V_{DS} = 20V, I_D = 20A V_{GS} = 10V	-	39	-	nC
Gate-Source Charge	Q_{gs}		-	11	-	nC
Gate-Drain Charge	Q_{gd}		-	7.5	-	nC
Drain-Source Diode Characteristics [7]						
Body Diode Reverse Recovery Time	t_{rr}	I_F = 20A, Vr=30V,dI/dt = 100A/μs, T_J = 25°C	-	51	-	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	47	-	nC
Diode Forward Current	I_S	T_C = 25°C	-	-	108	A

Notes:

1. This current is chip limited, whiich is calculated based on Rthjc.
2. This current is calculated on single pulse with 10μs Pulse & Duty Cycle = 1%.
3. Device mounted on FR-4 substrate PC board with 2oz copper in 1inch square cooling area.
4. Thermal resistance from junction to soldering point (on the exposed drain pad).
5. Short duration pulse test used to minimize self-heating effect.
6. Defined by design, not subject to production.

图 1. 输出特性

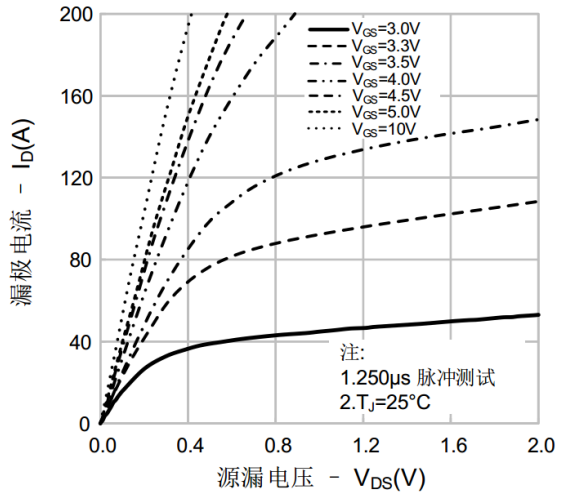


图 2. 传输特性

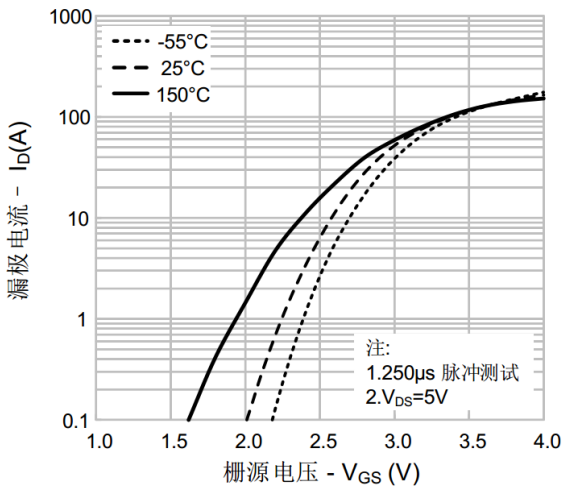


图 3. 导通电阻 vs. 漏极电流

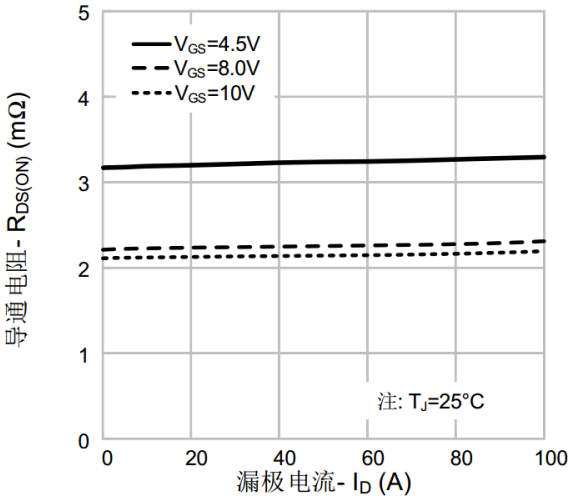


图 4.导通电阻 vs. 栅源电压

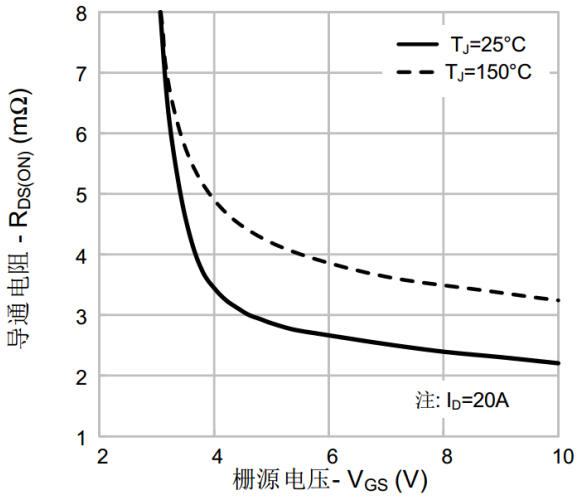


图 5. 开启电压 vs. 温度特性

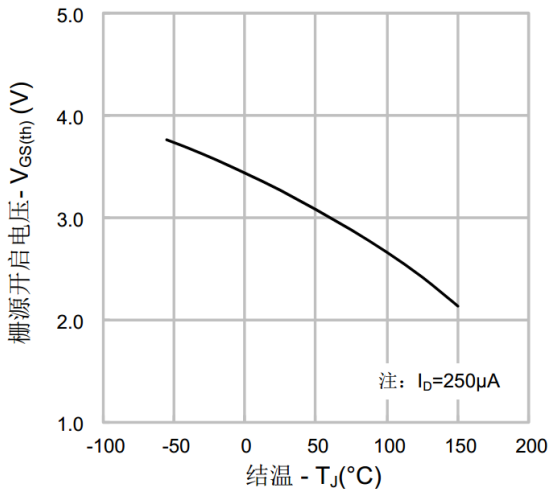


图 6. 体二极管正向压降 vs. 源极电流和温度

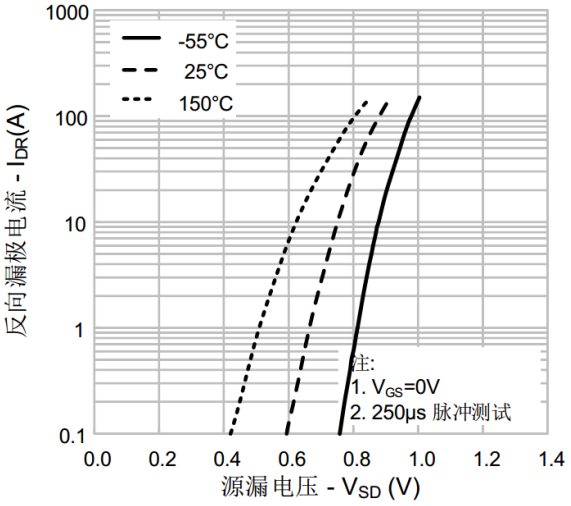


图 7.电容特性

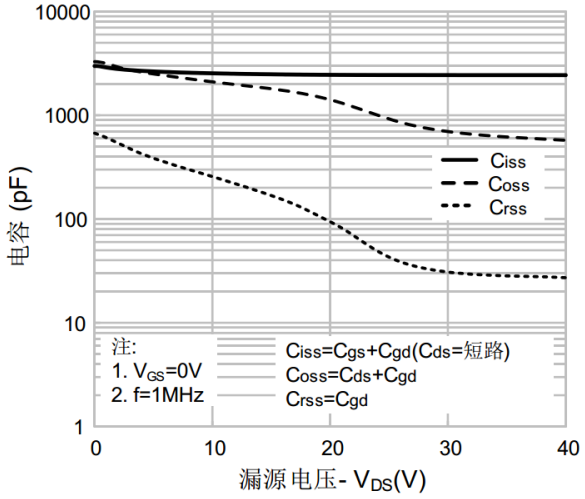


图 8. 电荷量特性

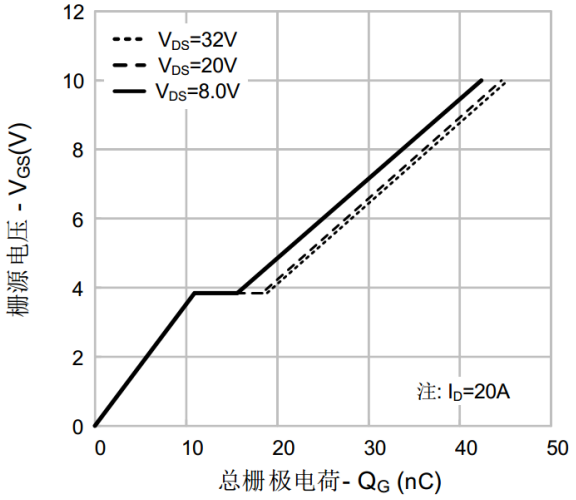


图 9. 击穿电压 vs. 温度

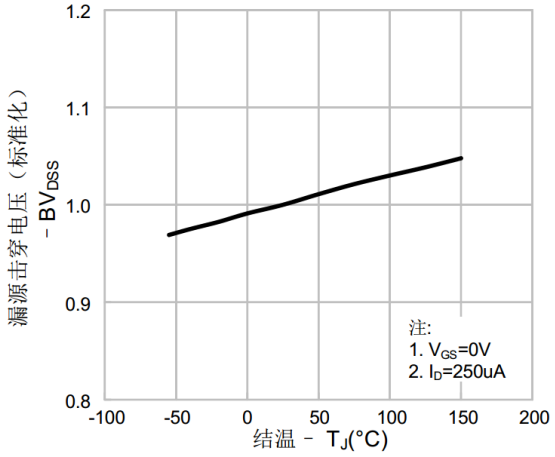


图 10. 导通电阻 vs. 温度

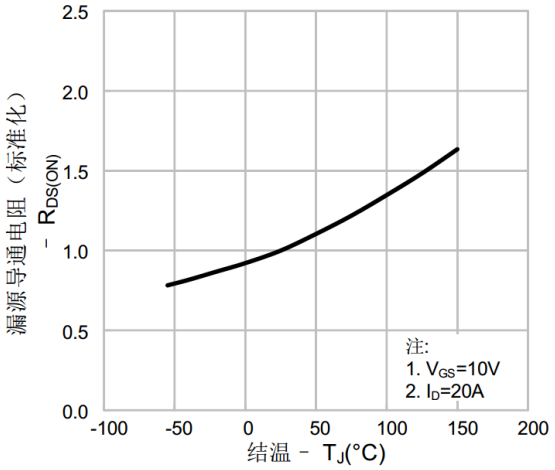


图11. 最大安全工作区域

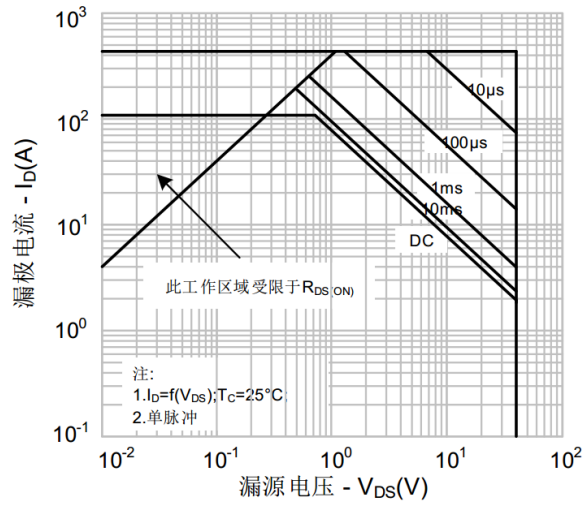


图 12. 耗散功率 vs. 温度

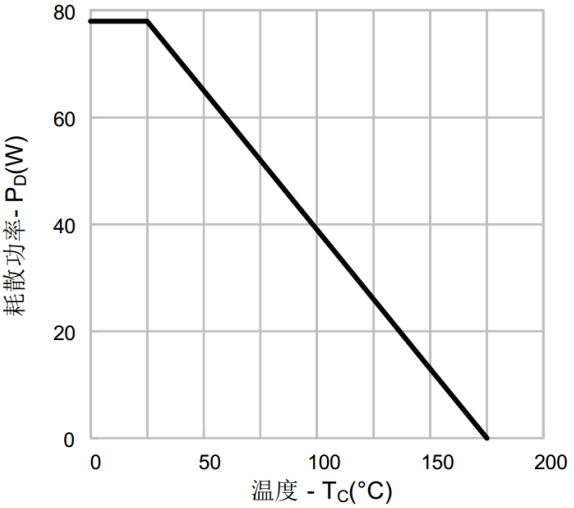


图13. 漏极电流 vs. 壳温

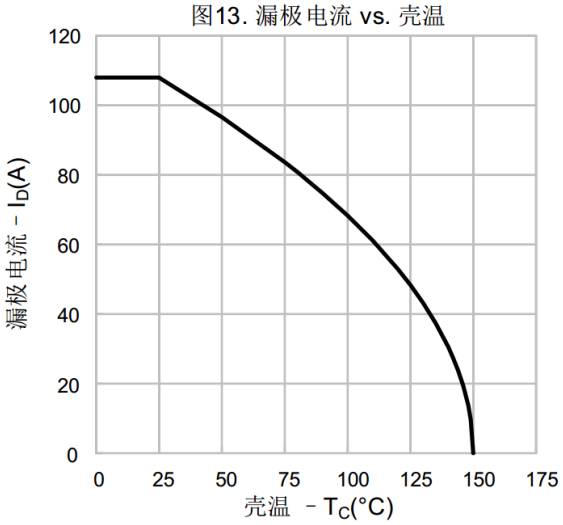
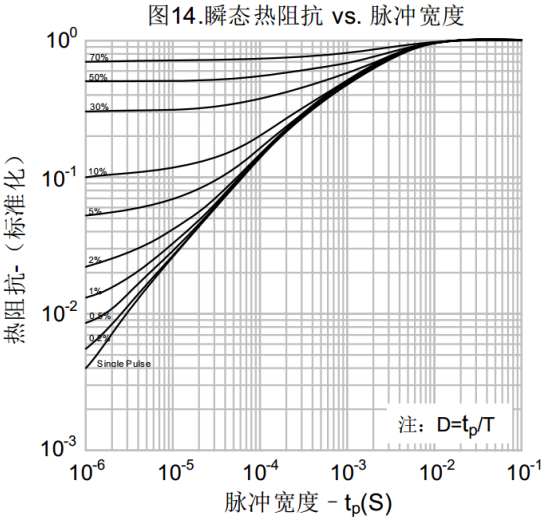


图14.瞬态热阻抗 vs. 脉冲宽度



Test Circuit and Waveform

Figure A: Gate Charge Test Circuit and Waveform

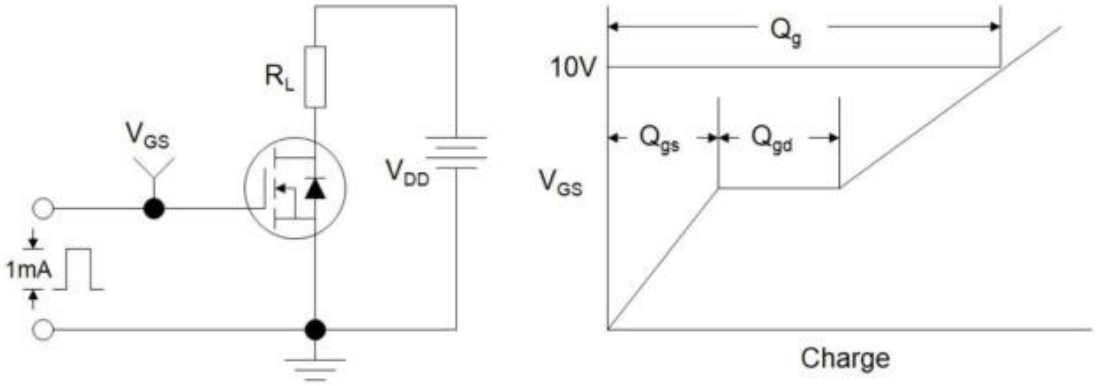


Figure B: Resistive Switching Test Circuit and Waveform

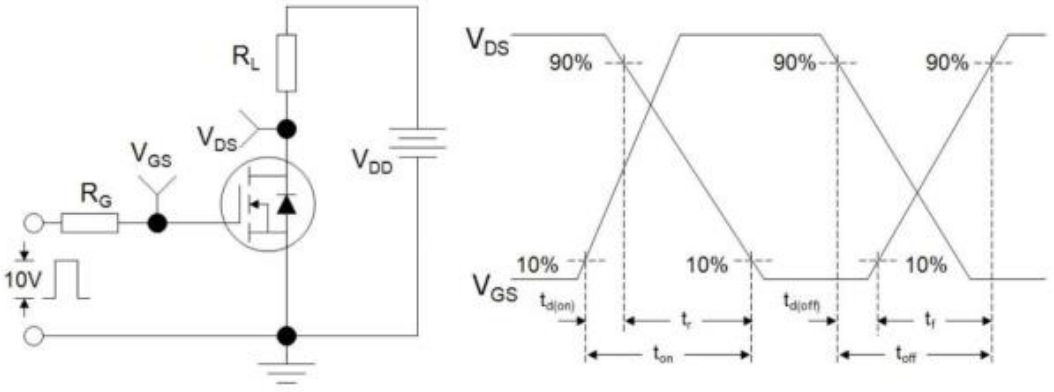
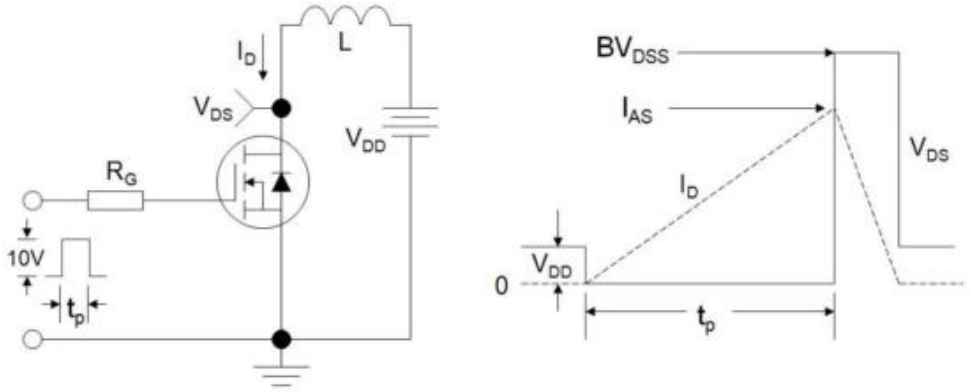
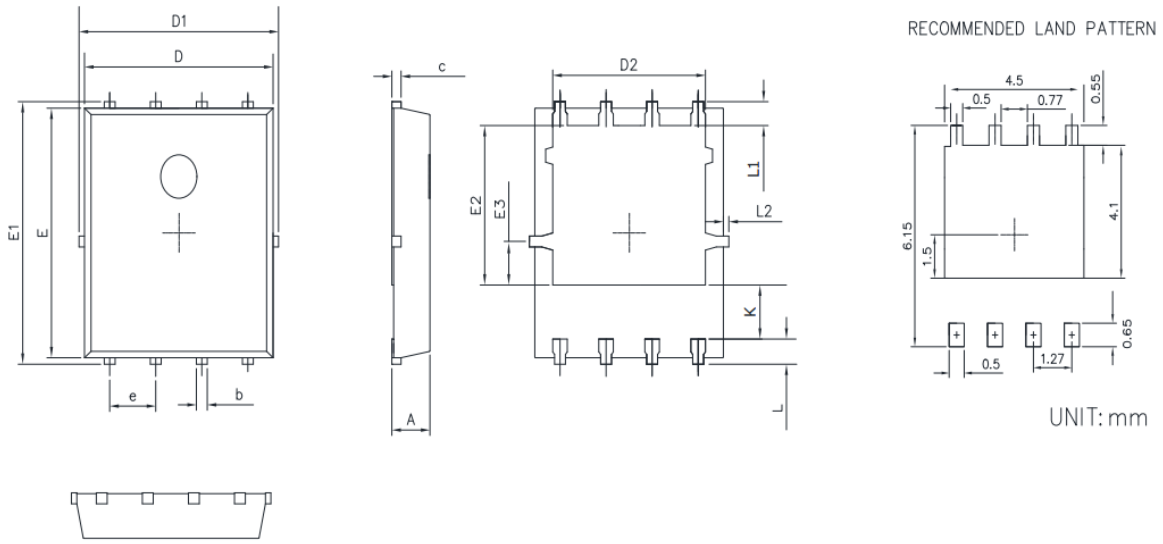


Figure C: Unclamped Inductive Switching Test Circuit and Waveform



Package Outline: DFN5X6



SYMBOL	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.90	1.10	0.035	0.043
b	0.25	0.50	0.010	0.020
c	0.10	0.30	0.004	0.012
D	4.80	5.30	0.189	0.209
D1	4.90	5.50	0.193	0.217
D2	3.92	4.20	0.154	0.165
E	5.65	5.85	0.222	0.230
E1	5.90	6.20	0.232	0.244
E2	3.33	3.78	0.131	0.149
E3	0.80	1.00	0.031	0.039
e	1.27		0.050	
L	0.40	0.70	0.016	0.028
L1	0.65		0.026	
L2	0.00	0.15	0.000	0.006
K	1.00	1.50	0.039	0.059