General description

The LMX5069TS15 high-side N_FET driver works with an internal MOSFET and acts as hot swap circuit with power limiting and over current protection function. The LMX5069TS15 is designed to control the in-rush current to the load upon insertion of a circuit card into a live backplane or other hot power source, thereby limiting the voltage sag on the backplane's supply voltage and the dv/dt of the voltage applied to the load.

The current limit in the internal series pass N-Channel MOSFET is programmable. The input undervoltage lockout levels are programmable by resistance divider networks. The LMX5069TS15 automatically restarts at a fixed duty cycle programmed by the Timer capacitor.

LMX5069TS15 is available in 14-pin eTSSOP package.

Features

♦ Wide operating range: 9V to 80V

♦ Adjustable current limit

♦ Circuit breaker function for severe overcurrent events

♦ Internal high side charge pump and gate driver for N-channel MOSFET

♦ Adjustable undervoltage lockout (UVLO)

♦ Available with automatic restart

♦ 14-Pin TSSOP package

Applications

♦ Server backplane systems

♦ Base station power distribution systems

♦ 12-60V Industrial systems

♦ POE protection circuit

♦ Solid state circuit breaker

General information

Ordering information

Part Number	Description
LMX5069TS15	eTSSOP14
MPQ	3000pcs

Package dissipation rating

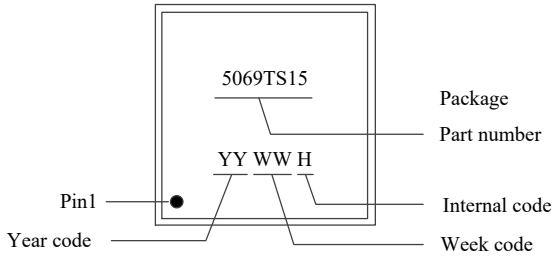
Package	RθJA（℃/W）
eTSSOP14	50

Absolute maximum ratings

Parameter	Value
VIN to GND	-0.3 to 100V
SENSE, OUT to GND	-0.3 to 100V
OUT to GND (1ms transient)	-0.3 to 100V
PWR, Timer to GND	-0.3 to 6.8V
VIN to SENSE	-0.3 to 0.3V
Maximum junction temperature, T_{JMAX}	150℃
Storage temperature, T_{stg}	-65 to 150℃

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

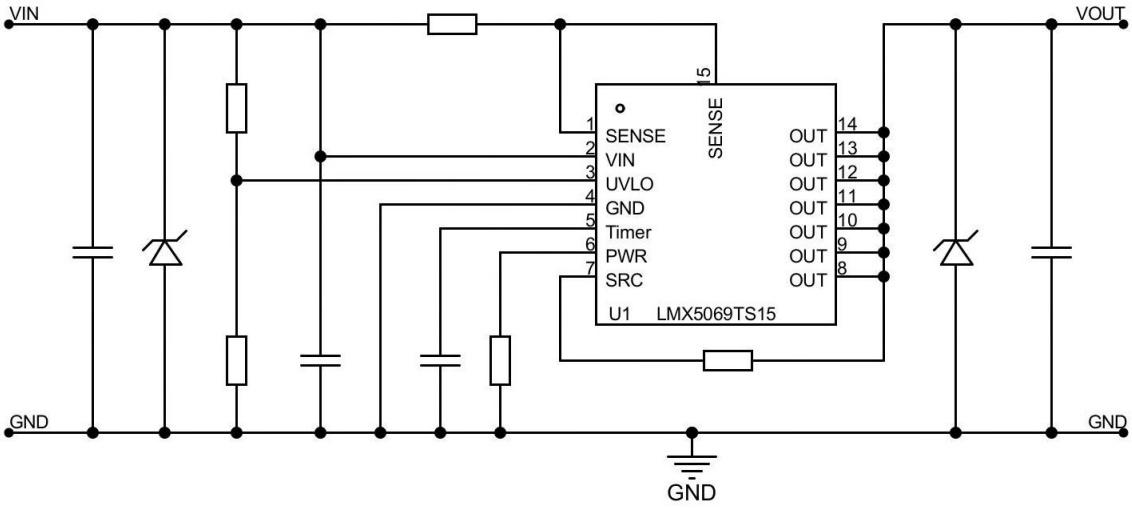
Marking information



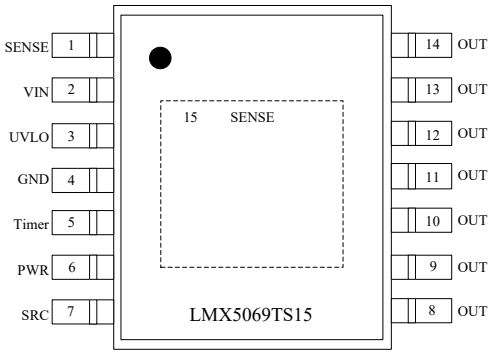
Recommended operating condition

Symbol	Range
Supply voltage	9 to 80V
PWR, Timer voltage	0 to 5V
Junction temperature	-40 to 125℃

Typical application

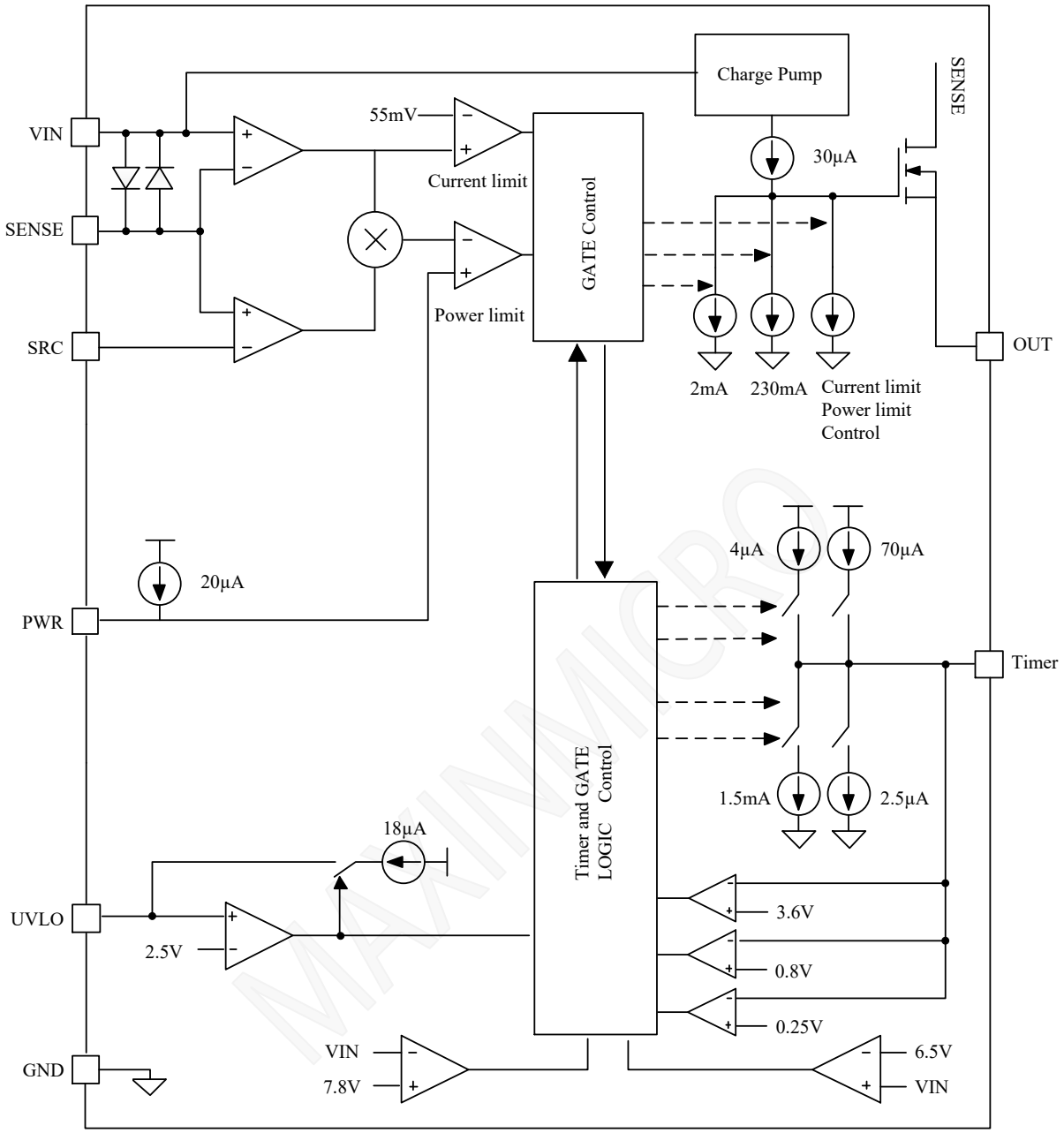


Terminal assignments



PIN num	PIN name	Description
1/15	**SENSE**	Current sense input: The voltage across the current sense resistor is measured from VIN to this pin. If the voltage across the R reaches 55mV(typical) the load current is limited and the fault timer activates.
2	**VIN**	Positive supply input: A small ceramic bypass capacitor close to this pin is recommended to suppress transients which occur when the load current is switched off.
3	**UVLO**	This is a dual function control pin. When used as an ENABLE pin and pulled down, it shuts off the internal pass MOSFET. As an UVLO pin, it can be used to program different UVLO trip point via external resistor divider.
4	**GND**	Circuit ground.
5	**Timer**	Timing capacitor: An external capacitor connected to this pin sets the insertion time delay and the fault timeout period. The capacitor also sets the restart timing.
6	**PWR**	Current limit set: An external resistor connected to this pin, in conjunction with the current sense resistor, sets the maximum power dissipation allowed in the external series pass MOSFET.
7	**SRC**	Output feedback: Connect to the output rail (internal MOSFET source). Internally used to determine the MOSFET VDS voltage for power limiting. Connect this pin to OUT across a resistor, and a 100R is recommended.
8-14	**OUT**	System OUT pin.

Block diagram



Electrical characteristics

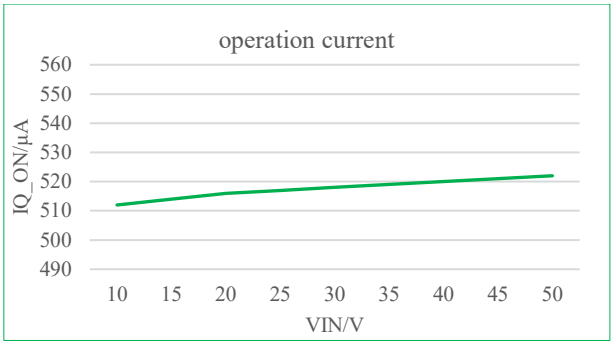
VIN = 24-48V, T_J = 25°C, unless otherwise noted.

Symbol	Parameters	Test conditions	Min	Typ	Max	Unit
INPUT (VIN PIN)						
VIN			9		80	V
IQ_{ON}	Supply current	UVLO>2.5V		450		μA
IQ_{OFF}		UVLO<2.5V	0		25	μA
V_{INSERT}			5.5	6.5	7.5	V
V_{INEN}			6.8		8.5	V
UVLO						
V_{UVLOR}	UVLO Threshold voltage	falling	2.25	2.5	2.75	V
$UVLO_{HYS}$	UVLO hysteresis current	UVLO=1V	12	18	24	μA
$UVLO_{BIAS}$	UVLO bias current	UVLO=48V			1	μA
OUT PIN						
I_{OUT_DIS}	OUT bias current, disabled	Disabled, OUT = 0V, SENSE = VIN		50		μA
I_{OUT_EN}	OUT bias current, enabled	Enabled, OUT=VIN		11		μA
PWR						
PWR_{ILM-1}	Power limit sense voltage (VIN-SENSE)	SEN-OUT=48V，RPWR=150kΩ	19	25	31	mV
PWR_{ILM-2}		SENSE-OUT=24V，RPWR=75 kΩ		25		mV
I_{PWR}	Power pin current	PWR=2.5V	17	20	23	μA
CURRENT LIMIT						
V_{CL}	Over current threshold	VIN-VSENSE	47	55	65	mV
I_{SENSE}	SENSE input current	Enable, OUT=SENSE		8		μA
		Disable, OUT=0V		10		μA
TIMER						
V_{TMRH}	Upper threshold	End of insertion time	3.2	3.6	4.0	V
V_{TMRL}	Lower threshold	Restart cycles	0.5	0.8	1.1	V
		End of 8th cycles		0.25		V
I_{TIMER}	Insertion time current	VIN=V_{INSERT}	2	4	6	μA
	Sink current, end of insertion time	Timer=2V	0.7		2	mA
	Fault detection current		45	70	95	μA
	Fault sink current		1.25	2.5	3.75	μA
DT_{FAULT}	Fault restart duty cycle			0.5		%
MOSFET						
VDS	Drain to Source voltage		100			V
Ron	On resistance	Vgs=10V		15		mΩ

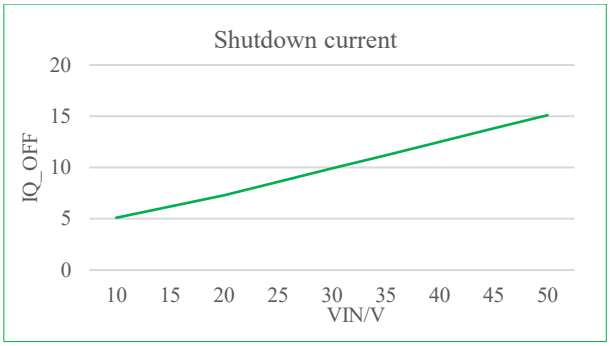
Timing characteristics

UVLO Timing						
$UVLO_{DLY}$	UVLO delay	UVLO rising to internal GATE begin to rise		55		μs
		UVLO falling to internal GATE begin to fall		20		μs
Current Limit Timing						
T_{CL}	Response time for OCP	VIN-SENSE stepped from 0V to 80mV		50		μs

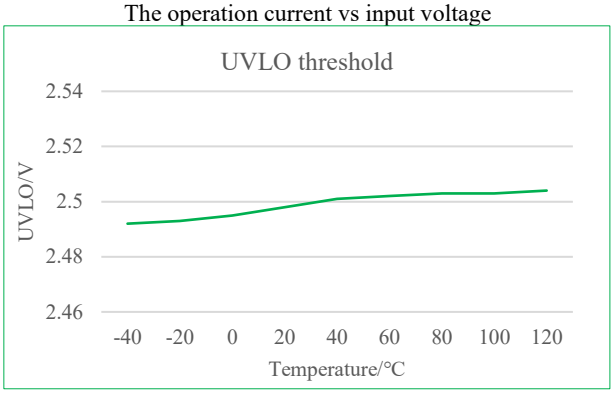
Characteristic plot (12-48V typical)



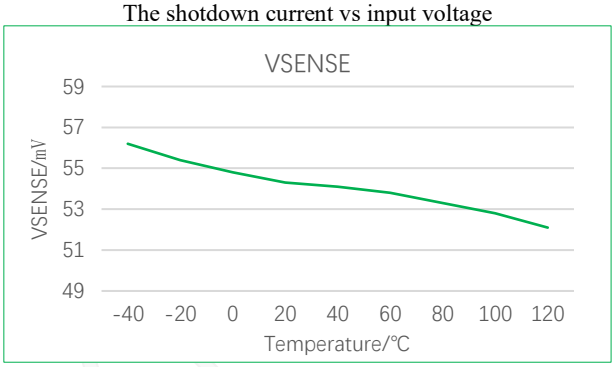
The operation current vs input voltage



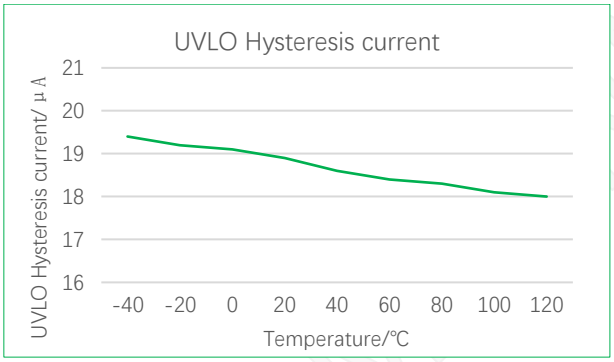
The shotdown current vs input voltage



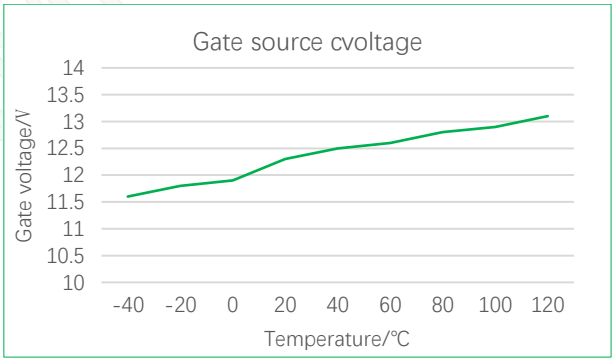
UVLO threshold vs temperature



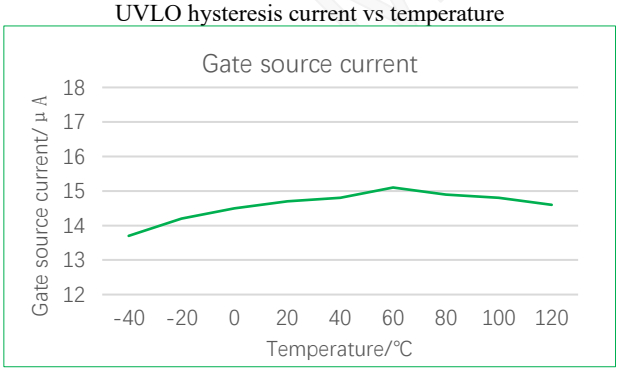
Current limit sense voltage vs temperature



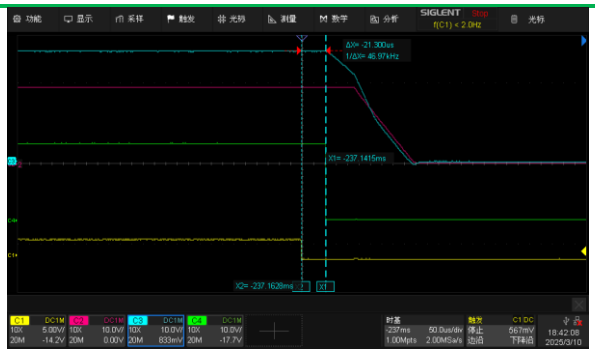
UVLO hysteresis current vs temperature



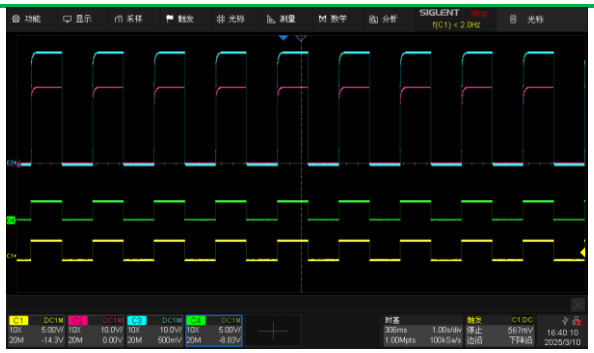
GATE to source voltaget vs temperature



GATE source current vs temperature

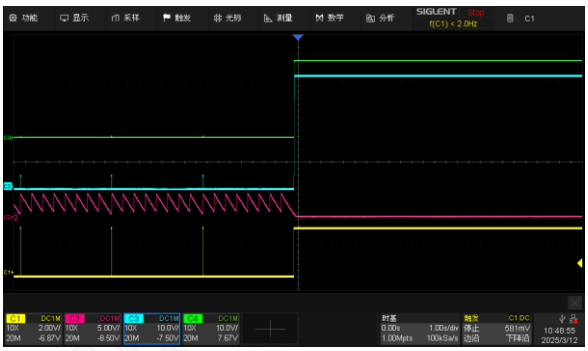


UVLO protection



Continues repeated switch on an off with 3A load

Over current protection



Over current release

Short circuit protection

Detailed description

Overview

LMX5069TS15 have programmable current limit, current limiting for an extended period results in the shutdown of the series pass device. In this event, the LMX5069TS15 retries an infinite number of times to recover after the fault is removed. The circuit breaker function quickly switches off the series pass device upon detection of a severe overcurrent condition. Programmable undervoltage lockout (UVLO) circuits shut down the LMX5069TS15 when the system input voltage is outside the desired operating range.

In addition to a programmable current limit, the LMX5069TS15 monitors and limits the maximum power dissipation in the series pass device to maintain operation with in the device Safe Operation Area. Either current limiting or power limiting for an extended period of time results in the shutdown of the series pass device. In this event, the LMX5069TS15 retries an infinite number of times to recover after the fault is removed. The circuit breaker function quickly switches off the series pass device upon detection of a severe overcurrent condition.

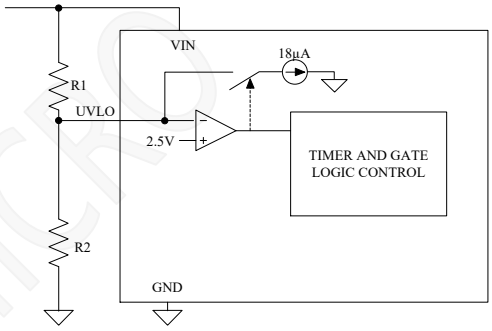
Undervoltage Lockout (UVLO)

The series pass MOSFET is enabled when the input supply voltage is within the operating range defined by the programmable undervoltage lockout levels. Typically the UVLO level at VIN is set with a resistor divider as shown in the figure below. When VIN is below the UVLO level, the internal 21μA current source at UVLO is enabled, the current source at OVLO is off, and OUT is break off. As VIN is increased, raising the voltage at UVLO above 2.5V, the 21μA current source at UVLO is switched off, increasing the voltage at UVLO, providing hysteresis for this threshold. With the UVLO pin above 2.5V, OUT is switched on by 30μA current source at the GATE pin if the insertion time delay has expired. The minimum possible UVLO level at VIN can be set by connecting the UVLO pin to VIN. In this case OUT is enabled when the VIN voltage reaches the V_{INEN} threshold.

There are two methods to configure UVLO to set the hysteresis threshold.

Option A

If all two thresholds must be accurately defined, the following figure can be used.



The two resistor values are calculated as follows:

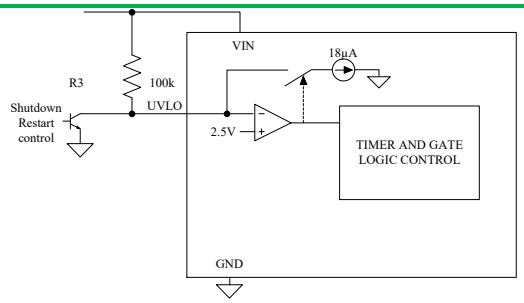
Choose the upper UVLO threshold (V_{UVH}) and lower UVLO threshold (V_{UVL}) with Equation5 and Equation6.

$$R1 = \frac{V_{UVH}-V_{UVL}}{18\mu A} = \frac{V_{UV(HYS)}}{18\mu A} \quad (5)$$

$$R2 = \frac{2.5V \times R1}{V_{UVL}-2.5V} \quad (6)$$

Option B

The minimum UVLO level is obtained by connecting the UVLO pin to VIN as shown in the following figure. Q1 is switched on when the VIN voltage reaches V_{INEN} threshold. An external transistor can be connected to UVLO to provide remote shutdown control.



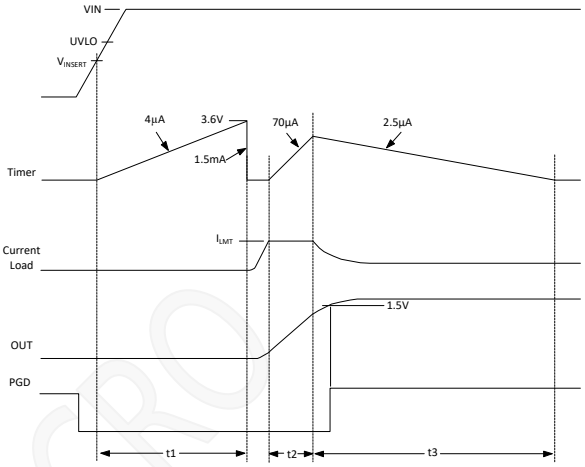
Power up sequence

The VIN operating range of the LMX5069TS15 is 9V to 80V. As the VIN initially increases, the internal NMOSFET is held off an 230mA pulldown current at the internal GATE. The strong pulldown current at the GATE pin prevents an inadvertent turn on as the MOSFET's gate to drain capacitance is charged. Additionally, the Timer pin is initially held at ground. When the VIN voltage reaches the VINSERT threshold the insertion time begins. During the insertion time, the capacitor at the Timer pin is charged by a 4µA current source, and internal MOS is held off by a 2mA pulldown current at the internal GATE regardless of the VIN voltage. The insertion time delay allows ringing and transient at VIN to settle before MOS can be enabled.

The insertion time ends when the Timer pin voltage reaches 3.6V. The capacitor is the quickly discharged by an internal 1.5mA pulldown current. After the insertion time, the LMX5069TS15 control circuity is enabled when VIN reaches the VINEN threshold. The internal power pass is switched on when VIN exceeds the UVLO threshold. If VIN is above the UVLO threshold at the end of the insertion time, OUT switches on at that time.

As the voltage at the OUT pin increases, the LMX5069TS15 monitors the drain current and power dissipation of MOSFET. In rush current limiting and power limiting circuits actively control the current delivered to the load. During the in rush limiting interval an internal 70µA fault timer current source charges the timer capacitor. If the power dissipation and the input current reduce below their respective limiting threshold before the Timer pin reaches 3.6V, the current 70µA source is switched off, and the capacitor is discharged by the internal 2.5µA current sink.

The Timer pin voltage 3.6V before in rush current limiting or power limiting ceases, a fault is declared and OUT is turned off.

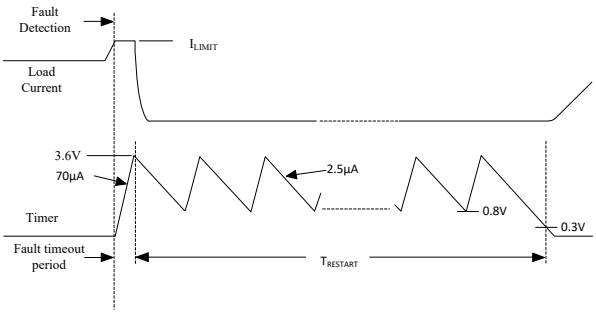


Fault timer and restart

When the current limit or power limit threshold is reached during turn on or as result of a fault condition, the internal gate to source voltage is modulated to regulate the load current and power dissipation. When either function is activated, an 70µA fault timer current source charged the external capacitor at the Timer pin. If the fault condition subsides during the fault timeout period before the Timer pin reaches 3.6V, the LMX5069TS15 returns to the normal operating mode and the Timer capacitor is discharged by the 2.5µA current sink. If the Timer pin reaches 3.6V during the fault timeout period, OUT will be switched off .

The LMX5069TS15 provides an automatic restart sequence which consists of the Timer pin cycling between 3.6V and 0.8V seven times after the fault timeout period as shown in the following figure. The period of each cycle is determined by the 70µA charging current, and the 2.5µA discharging current, and the value of the capacitor at Timer pin. When the Timer pin reaches 0.3V during the eight high to low ramp,

the OUT will be switched on. If the fault condition is still present, the fault timeout period and the restart cycle repeat.



The fault timer runs when the hot swap is in power limit or current limit, which is the case during start up. Thus the timer has to be sized large enough to prevent a time out during start up. If the part starts directly into current limit the maximum start time can be computed with Equation9.

$$t_{start,max} = \frac{C_{OUT} \times V_{INMAX}}{I_{LIM}} \quad (9)$$

For most designs, $I_{LIM} \times V_{DS} > P_{LIM}$, so the hot swap starts in power limit and transition into current limit. In that case, the estimated start time can be computed with Equation10.

$$t_{start} = \frac{C_{OUT}}{2} \times \left(\frac{V_{INMAX}^2}{P_{LIM}} + \frac{P_{LIM}}{I_{LIM}^2} \right) \quad (10)$$

Note that the above start time assumes constant, typical current limit and power limit values. The actual start up time is slightly longer, as the power limit is a function of VDS and decreases as the output voltage increases. To ensure that the timer never times out during start up, we recommend setting the minimum fault time to be greater than the start up time by adding an additional 50% of the fault time. This accounts for the variation in power limit, timer current and timer capacitance. Thus the charge time can be computed with Equation11.

$$t_{FLT} = \frac{C_{Timer} \times 3.6V(typ)}{70\mu A(typ)} \quad (11)$$

Current Limit

The current limit threshold reached when the voltage across the sense resistor Rs (VIN to SENSE) reaches 55mV. In the current limiting condition, the internal GATE voltage is controlled to limit the current in pass MOSFET. While the current limit circuit is active, the fault SST is active. If the load current falls below the current limit threshold before the end of the fault timeout period. For proper operation, the RS resistor value must be no larger than 100mΩ.

Power limit

An important feature of the LMX5069TS15 is the power limit. The power limit function can be used to maintain the maximum power dissipation of internal MOSFET within the device SOA rating. The LMX5069TS15 determines the power dissipation in MOSFET by monitoring its drain to source voltage, and the drain current through the sense resistor. The product of the current and voltage is compared to the power limit threshold programmed by the resistor at the PWR pin. If the power dissipation reaches the limiting circuit is active.

In general, a lower power limit setting is preferred to reduce the stress on the MOSFET. However, when the LMX5069TS15 is set to a very low power limit setting, it has to regulate the FET current and hence the voltage across the sense resistor to a very low value. V_{SENSE} can be computed as shown in Equation12.

$$V_{SENSE} = \frac{P_{LIM} \times R_{SENSE}}{V_{DS}} \quad (12)$$

To avoid significant degradation of the power limiting accuracy, a V_{SENSE} of less than 5mV is not recommended. Based on this requirement the minimum allowed power limit can be computed in Equation13.

$$P_{ILIMMIM} = \frac{V_{SENSEMIN} \times V_{INMAX}}{R_{SENSE}} = \frac{5mV \times V_{INMAX}}{R_{SENSE}} \quad (13)$$

Note that the minimum R_{PWR} would occur when $V_{DS}=V_{INMAX}$. We can then compute the minimum R_{PWR} with Equation14.

$$R_{PWR} = 180000 \times R_{SENSE} \left(P_{LIM} - 1.0mV \times \frac{V_{INMAX}}{R_{SENSE}} \right) \quad (14)$$

As the designed MOSFET integrated, the Timer capacitor and PWR resistor can reference the following table.

Rsense=10mΩ		
Iocp=5.5A typical		
Timer	Debounce time	PWR
200nF	10ms	⩽39kΩ
100nF	5ms	⩽62kΩ
10nF	1ms	⩽120kΩ
1nF	0.1ms	⩽500kΩ

Rsense=25mΩ		
Iocp=2.2A		
Timer	Debounce time	PWR
200nF	10ms	⩽22kΩ
100nF	5ms	⩽30kΩ
10nF	1ms	⩽90kΩ
1nF	0.1ms	⩽360kΩ

Input and Output Protection

Proper operation of the LMX5069TS15 hot swap circuit requires a voltage clamping element present on the supply side of the connector into which the hot swap circuit is plugged in. A TVS is ideal, as depicted in Typical application. The TVS is necessary to absorb the voltage transient generated whenever the hot swap circuit shuts off the load current. This effect is the most severe during a hot-short when a large current is suddenly interrupted when the FET shuts off. The TVS must be chosen to have minimal leakage current at V_{INMAX} and to clamp the voltage to under 30V during hot-short events. A 100~200ohm resistor should be placed between OUT pin and Source of external MOSFET to prevent damage from surge voltage, as the R_{SOURCE} shown in the Typical application.

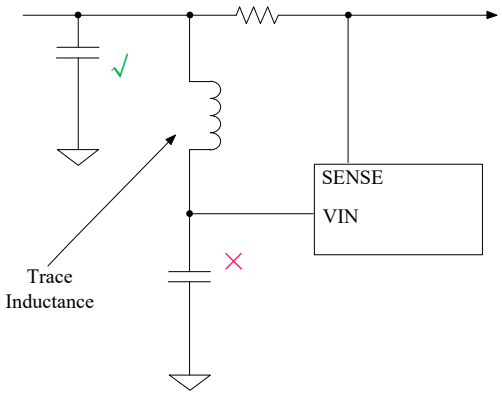
Power Supply Recommendations

In general, the LMX5069TS15 behavior is more reliable if it is supplied from a very regulated power supply. However, high-frequency transients on a backplane are not uncommon due to adjacent card insertions or faults. If this is expected in the end system, Maxin recommends placing a 1μF ceramic capacitor to ground close to the drain of the hot swap MOSFET. This reduces the common mode voltage seen by VIN and SENSE. Additional filtering may be necessary to avoid nuisance trips.

Layout Guidelines

The following guidelines must be followed when designing the PC board for the LMX5069TS15:

- Place the LMX5069TS15 close to the board's input connector to minimize trace inductance from the connector to the FET.
- Note that special care must be taken when placing the bypass capacitor for the VIN pin. During hot shorts, there is a very large dv/dt on input voltage after the MOSFET turns off. If the bypass capacitor is placed right next to the pin and the trace from R_{SENSE} to the pin is long, an LC filter is formed. As a result, a large differential voltage can develop between VIN and SENSE. To avoid this, place the bypass capacitor close to R_{SENSE} instead of the VIN pin.



Layout Trace Inductance

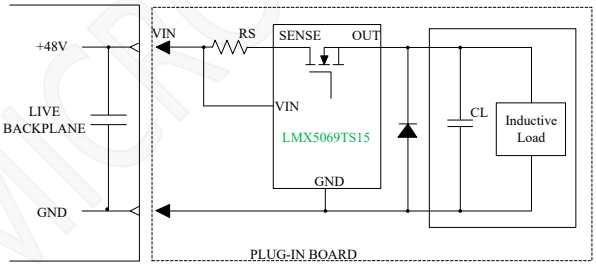
- The sense resistor (R_S) must be close to the LMX5069TS15, and connected to it using the Kelvin techniques.
- The high current path from the board's input to the load (via Q1), and the return path, must be parallel and close to each other to minimize loop inductance.

- The ground connection for the various components around the LMX5069TS15 must be connected directly to each other, and to the LMX5069TS15's GND pin, and then connected to the system ground at one point. Do not connect the various component grounds to each other through the high current ground line.
- Provide adequate heat sinking for the series pass device (Q1) to help reduce stresses during turn on and turn off.
- The board's edge connector can be designed to shut off the LMX5069TS15 as the board is removed, before the supply voltage is disconnected from the LMX5069TS15. When the board is inserted into the edge connector, the system voltage is applied to the LMX5069TS15's VIN pin before the UVLO voltage is taken high.

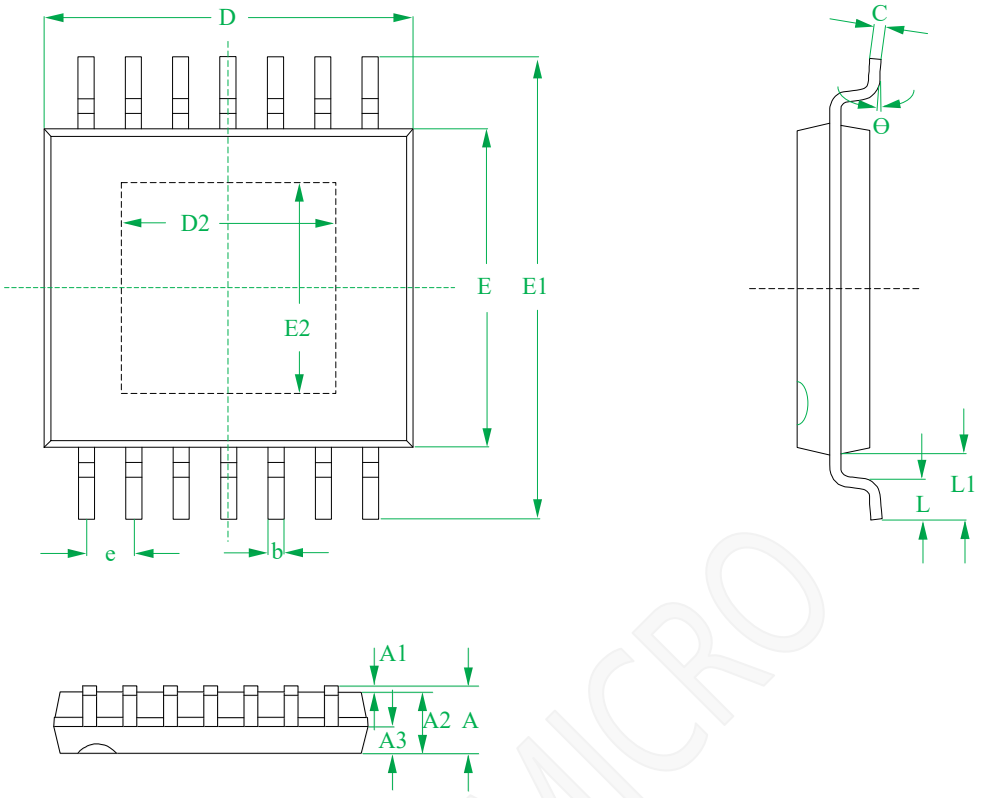
System Considerations

A) Continued proper operation of the LMX5069TS15 hot swap circuit requires capacitance to be present on the supply side of the connector into which the hot swap circuit is plugged in, as depicted in the following figure. The capacitor in the Live Backplane section is necessary to absorb the transient generated whenever the hot swap circuit shuts off the load current. If the capacitance is not present, inductance in the supply lines generates a transient voltage at shut-off which can exceed the absolute maximum rating of the LMX5069TS15, resulting in its destruction.

B) If the load powered via the LMX5069TS15 hot swap circuit has inductive characteristics, a diode is required across the LMX5069TS15's output. The diode provides a recirculating path for the load's current when the LMX5069TS15 shuts off that current. Adding the diode prevents possible damage to the LMX5069TS15 as the OUT pin is taken below ground by the inductive load at shutoff.



Package information eTSSOP14



ETSSOP14 for LMX5069TS15

SYMBOL	MILLIMETERS		
	MIN	NOM	MAX
A			1.20
A1	0.05	0.03	0.15
A2	0.90	1.00	1.05
A3	0.39	0.44	0.49
b	0.20		0.28
C	0.13		0.17
D	4.90	5.00	5.10
D2		2.95REF	
E	4.30	4.40	4.50
E1	6.20	6.40	6.60
E2		2.90REF	
e		0.65BSC	
L	0.45	0.60	0.75
L1		1.00REF	
θ	0°		8°

Restrictions on Product Use

◆ MAXIN micro is continually working to improve the quality and reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing MAXIN products, to comply with the standards of safety in making a safe design for the entire system, and to avoid situations in which a malfunction or failure of such MAXIN products could cause loss of human life, bodily injury or damage to property.

◆ In developing your designs, please ensure that MAXIN products are used within specified operating ranges as set forth in the most recent MAXIN products specifications.

◆ The information contained herein is subject to change without notice.

Version update record:

V10 The original version