General description

The MX5015D22 high-side N_FET driver works with an external MOSFET and acts as an ideal diode rectifier when connected in series with the power supply. This controller enables MOSFETs to replace diode rectifiers in power distribution networks, reducing power loss and voltage drop.

The MX5015D22 controller provides charge pump gate drive for an external N-channel MOSFET and fast response comparator to turn off the FET when current flows in reverse.

The MX5015D22 can be connected with a resistance divider network to achieve the input over voltage protection.

Features

- ♦ Wide operating input voltage range V_{IN}: 5V to 30V
- ♦60V transient voltage
- ♦ Charge pump gate driver for external N-channel MOSFET
- ♦ 50ns fast response to current reversal
- ♦2A peak gate off current
- ♦Ultra-small V_{DS} turn-off voltage reduces turn-off time
- ♦ 6-Pin SOT23-6L

Applications

Active OR-ing of redundant (N+1) power supplies

Pre-charge control

High side driver

Input OVP protection

General information

Ordering information

Part Number	Description
MX5015D22	DFN2*2
MPQ	3000pcs

Package dissipation rating

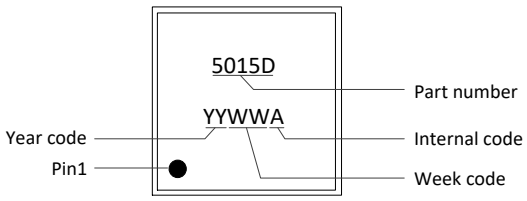
Package	RθJA（℃/W）
SOT-23 (6)	108.1

Absolute maximum ratings

Parameter	Value
VIN, SOURCE Pins to GND	-0.3 to 60V
GATE Pin to GND	-0.3 to 70V
EN Pin to Ground	-0.3 to 7V
OVP Pin to Ground	-0.3 to 7V
Junction temperature	150℃
Storage temperature, Tstg	-50 to 150℃
Leading temperature （soldering,10secs）	260℃
ESD Susceptibility HBM	±2000V

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

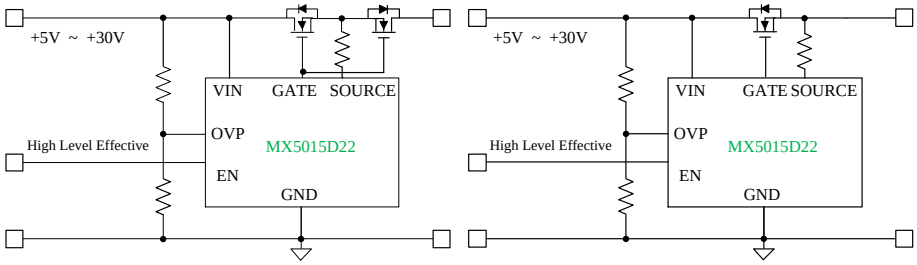
Marking information



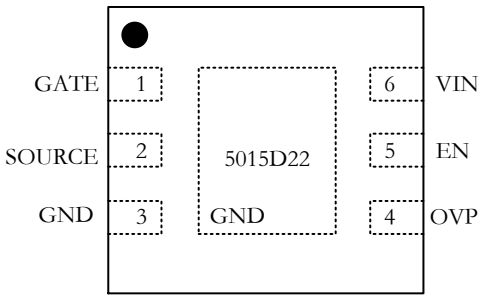
Recommended operating condition

Symbol	Range
VIN, OUT Pins	5-30V
EN, OVP Pin	0-5.5V
Operating temperature	-40~125℃

Typical application



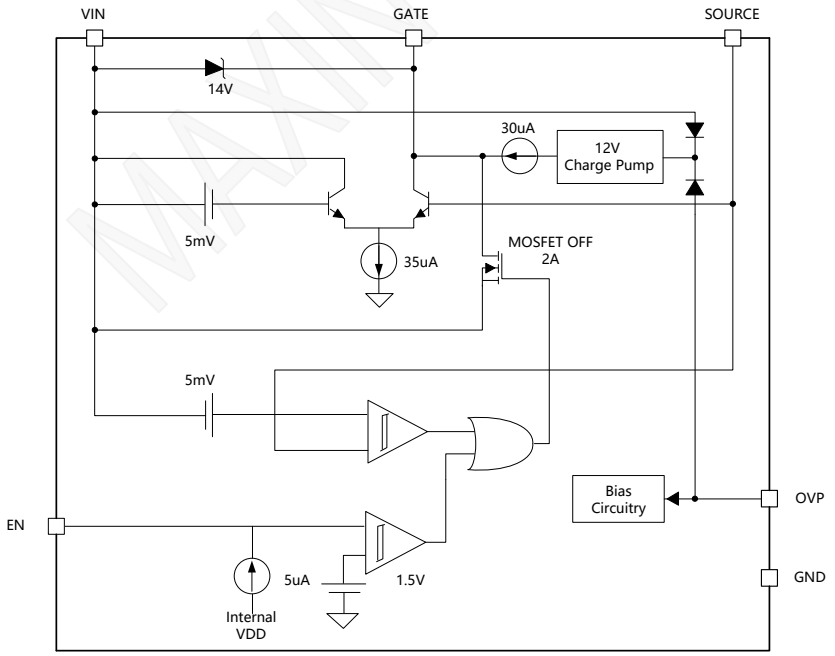
Terminal assignments



Pin information

PIN NO.	PIN name	Description
1	GATE	Connect to the Gate of the external MOSFET. Controls the MOSFET to emulate a low forward-voltage diode.
2	Source	Voltage sense connection to the external MOSFET source pin. This pin must connected a resistor between external MOSFET.
3	GND	Ground return for the controller
4	OVP	Input over voltage protection pin. When the voltage of OVP exceed 1.2V(typical), off the external MOSFET. Connected to GND when not used. This pin cannot be flaoting.
5	EN	External enabling pin. High level effective. This pin can be floating.
6	VIN	Input pin.
Thermal pad		GND

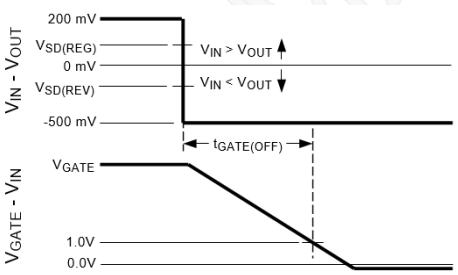
Block diagram



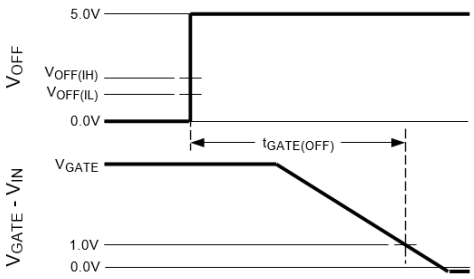
Electrical characteristics

（V_{IN} =12V, OVP=0V, T_A = 25℃, unless otherwise noted）

Symbol	Parameter	Test condition	Min	Typ.	Max	Unit
Supply current	V_{IN} = 30V	EN = Low	30	50	70	μA
		EN = High	180	280	380	μA
	V_{IN} = 12V	EN = Low	25	45	65	μA
		EN = High	180	280	380	μA
	V_{IN} = 5V	EN = Low	20	40	60	μA
		EN = High	160	260	360	μA
EN threshold	5.0V ≤ V_{IN} ≤ 30V	EN threshold, falling			1.10	V
		EN threshold, rising	2.10			V
EN current	5.0V ≤ V_{IN} ≤ 30V	EN = Low	-2.0		0	μA
		EN = High	-2.0	1.0	2.0	μA
EN capacitance				5.0		pF
OVP threshold	5.0V ≤ V_{IN} ≤ 30V	OVP threshold	1.16	1.22	1.30	V
		OVP recovery	1.00	1.18	1.22	V
Zener clamp V_{GATE} -V_{SOURCE}	5V ≤ V_{IN} ≤ 30V	EN = High	3.5	12	15	V
Gate turn on time for OVP	V_{IN} = 20V, C_L = 1nF, R_{SOURCE} = 100Ω	OVP = Low, measure time to Vgate = V_{IN} + 4V		1.02		ms
Gate turn off time for OVP	V_{IN} = 20V, C_L = 1nF, R_{SOURCE} = 100Ω	OVP = High, measure time to Vgate = 1V		1.12		us
Gate turn on time for EN	V_{IN} = 20V, C_L = 1nF, R_{SOURCE} = 100Ω	EN = High, measure time to Vgate = V_{IN} + 4V		1.12		us
Gate turn off time for EN	V_{IN} = 20V, C_L = 1nF, R_{SOURCE} = 100Ω	EN = Low, measure time to Vgate = 1V		960		ns
$V_{SD(REV)}$	Reverse V_{SD} Threshold V_{IN} < V_{OUT}	V_{IN} - V_{OUT}	-8	-5	-1	mV
$V_{SD(REG)}$	Regulated Forward V_{SD} Threshold V_{IN} > V_{OUT}	V_{IN} = 12V, V_{VS} = V_{IN}, V_{IN} - V_{OUT}	1	5	8	mV
$t_{SD(REG)}$	Gate turn off time for reverse	V_{IN} = 20V, I_O=3A, C_L = 1nF, R_{SOURCE} = 100Ω		3.12		us

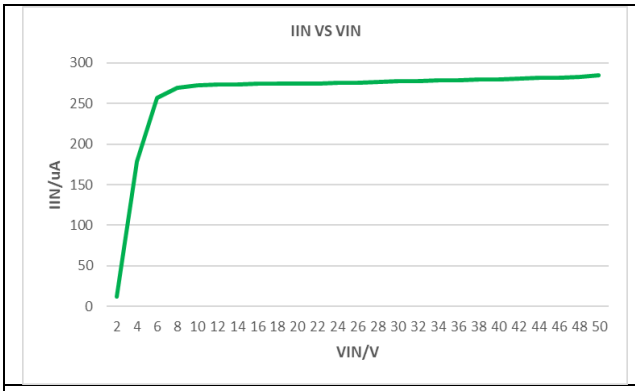


Gate OFF Timing for Forward to Reverse Transition

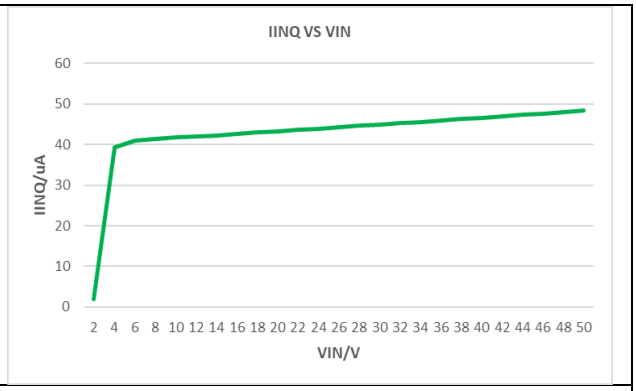


Gate OFF Timing for OFF Pin Low to High Transition

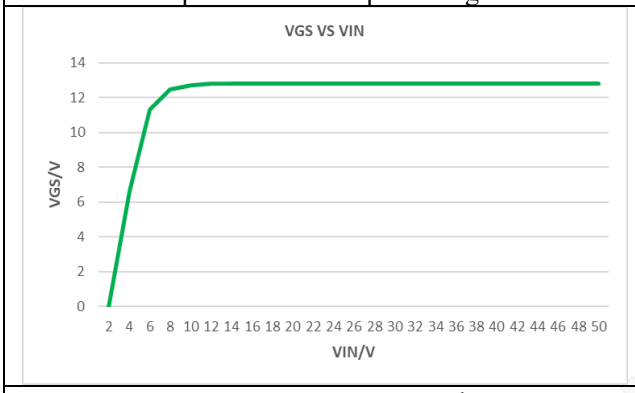
Characteristic plots



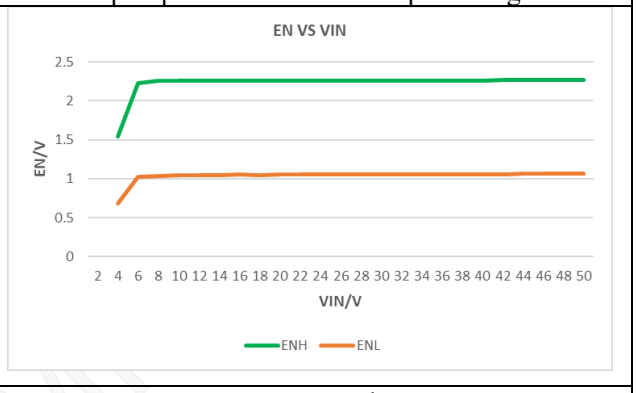
Input current vs Input voltage



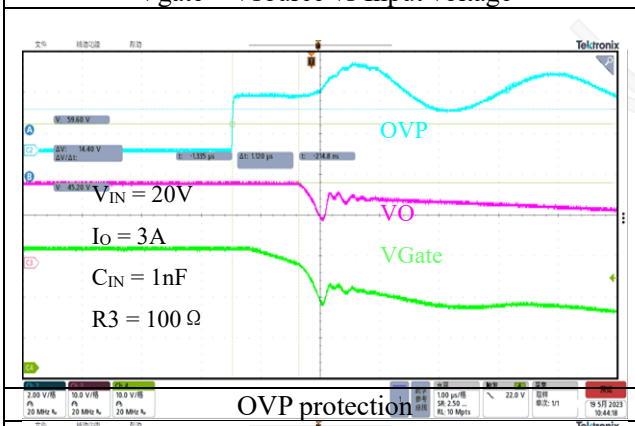
Input quiescent current vs Input voltage



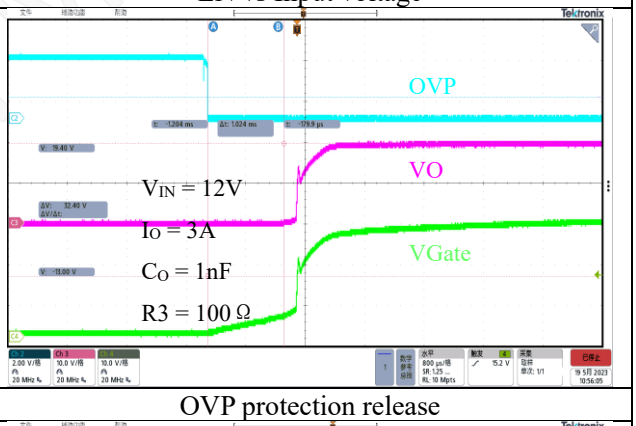
Vgate – Vsource vs Input voltage



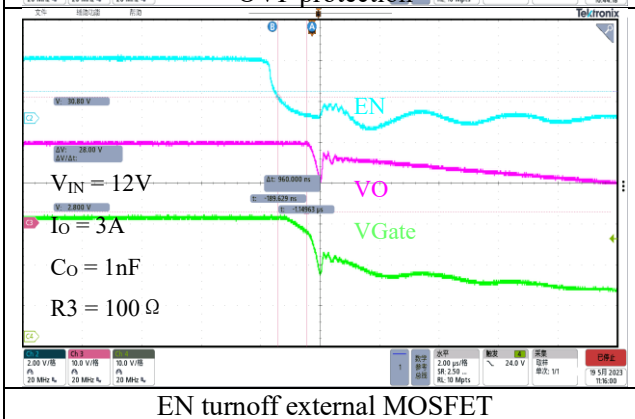
EN vs Input voltage



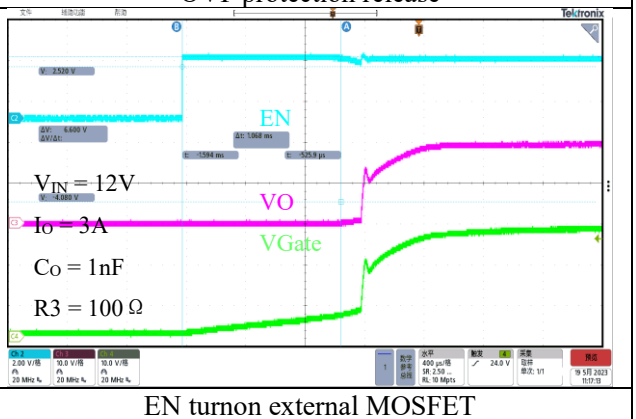
OVP protection



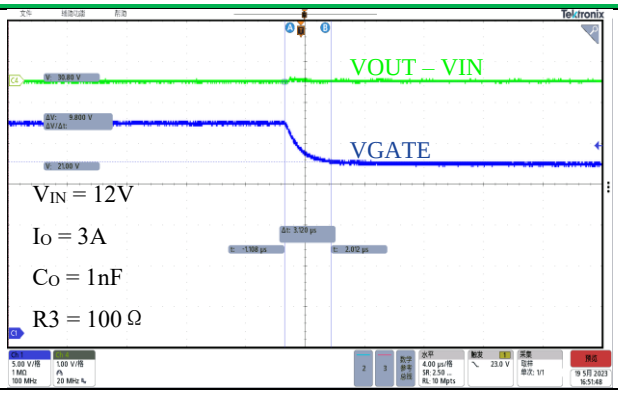
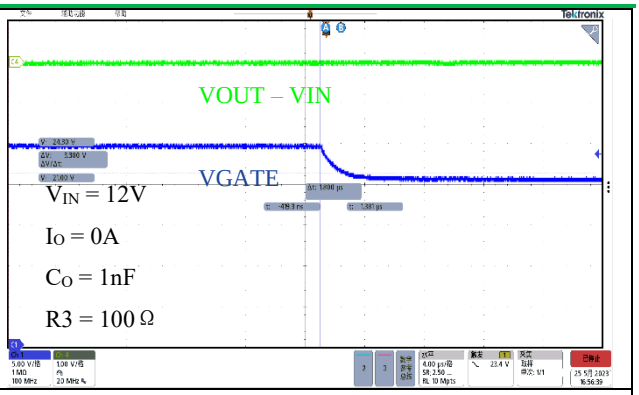
OVP protection release



EN turnoff external MOSFET



EN turnon external MOSFET

	
Reverse prtection	Reverse prtection

Operation description

The internal functions of these devices are controlled via a logic block connected to the EN pin. When the EN is off, all functions are turned off, and the gate of the external power MOSFET is held low via two N-channel switches. This results in a very low standby current, 40uA typical, which is necessary to power an internal bandgap. When the EN is driven to the "ON" state, the N-channel switches are turned off, the charge pump is turned on, and the P-channel switch between the charge pump and the gate turns on, allowing the gate of the power MOSFET to be charged. The op amp and internal Zener from an active regulator which shuts off the charge pump when the gate voltage is high enough.

The charge pump incorporates a 100kHz oscillator and on chip pump capacitors capable of charging a 1000pF load in 90us typical. In addition to providing active regulation, the internal 12V Zener is included to prevent exceeding the GS rating of the power MOSFET at high supply voltages.

The over voltage protection can be set by an external resistor divider between VIN, OVP and GND. When the voltage of OVP pin exceed the internal reference voltage (1.22V typical), An internal circuit will off the external FET to protect overvoltage. This pin cannot be floating.

The MX5015D22 devices have been improved for greater ruggedness and durability.

Construction Hints

High current pulse circuits demand equipment and assembly techniques that are more stringent than normal, low current lab practices. The following are the sources of pitfalls most often encountered during prototyping:

Supplies: Many bench power supplies have poor transient response. Circuits that are being pulse tested, or those that operate by pulse width modulation will produce strange results when used with a supply that has poor ripple rejection, or a peaked transient response. Always monitor the power supply voltage that appears at the drain of a high side driver (or the supply side of the load for a low side driver) with an oscilloscope. It is not uncommon to find bench power supplies in the 1kW class that overshoot or undershoot by as much as 50% when pulse loaded. Not only will the load current and voltage measurements be affected, but it is possible to overstress various components, especially electrolytic capacitors, with possible catastrophic results. A 10uF supply bypass capacitor at the chip is recommended.

Residual resistances: resistances in circuit connections may also cause confusing results. For example, a circuit may employ a 50mΩ power MOSFET for low voltage drop, but unless careful construction techniques are used, one could easily add 50 to 100mΩ resistance. Do not use a socket for the MOSFET. If the MOSFET is a TO-220 type package, make high current connections to the drain tab. Wiring losses have profound effect on high current circuits. A floating million meter can identify connections that are contributing excess drop under load.

Low voltage testing

As the MX5015D22 has relatively high output impedances, a normal oscilloscope probe will load the device. This is especially pronounced at low voltage operation. It is recommended that a FET probe or unity gain buffer be used for all testing.

Circuit topologies

The MX5015D22 is well suited for use with standard power MOSFETs in both low and high side driver configurations. In addition, the lower supply voltage requirements of these devices make them ideal for use with logic level FETs in high side applications with a supply 3 to 30V. In addition, a standard IGBT can be driven using these devices.

Choice of one topology over another is usually based on speed vs. safety. The fastest topology is the low side driver; however, it is not usually considered as safe as high side driving as it is easier to accidentally short a load to ground than to VIN. The slowest, but safest topology is the high side driver; with speed being inversely proportional to supply voltage. It is the preferred topology for most military and automotive applications. Speed can be improved considerably by bootstrapping from the supply.

MOSFET Selection

The important MOSFET electrical parameters are the maximum continuous Drain current I_D, the maximum Source current (that is, body diode) I_S, the maximum drain-to-source voltage $V_{DS(MAX)}$, the gate-to-source threshold voltage $V_{GS(TH)}$,

the drain-to-source reverse breakdown voltage $V_{(BR)DSS}$, and the drain-to-source on resistance $R_{DS(ON)}$.

The maximum continuous drain current, I_D, rating must exceed the maximum continuous load current. The rating for the maximum current through the body diode, I_S, is typically rated the same as, or slightly higher than the drain current, but body diode current only flows while the MOSFET gate is being charged to $V_{GS(TH)}$.

Gate Charge Time = Qg / $I_{GATE(ON)}$

1. The maximum drain-to-source voltage, $V_{DS(MAX)}$, must be high enough to withstand the highest differential voltage seen in the application. This would include any anticipated fault conditions.
2. The drain-to-source reverse breakdown voltage, $V_{(BR)DSS}$, may provide some transient protection to the OUT pin in low voltage applications by allowing conduction back to the IN pin during positive transients at the OUT pin.
3. The gate-to-source threshold voltage, $V_{GS(TH)}$, should be compatible with the MX5015D22 gate drive capabilities. Logic level MOSFETs, with $R_{DS(ON)}$ rated at $V_{GS(TH)}$ at 5V, are recommended, but sub-Logic level MOSFETs having $R_{DS(ON)}$ rated at $V_{GS(TH)}$ at 2.5V, can also be used.
4. The dominate MOSFET loss for the MX5015D22 active OR-ing controller is conduction loss due to source-to- drain current to the output load, and the $R_{DS(ON)}$ of the MOSFET. This conduction loss could be reduced by using a MOSFET with the lowest possible $R_{DS(ON)}$. However, contrary to popular belief, arbitrarily selecting a MOSFET based solely on having low $R_{DS(ON)}$ may not always give desirable results for several reasons:

1. Reverse transition detection. Higher $R_{DS(ON)}$ will provide increased voltage information to the MX5015D22 Reverse Comparator at a lower reverse current level. This will give an earlier MOSFET turnoff condition should the input voltage become shorted to ground. This will minimize any disturbance of the redundant bus.
2. Reverse current leakage. In cases where multiple input supplies are closely matched it may be possible for some small current to flow continuously through the MOSFET drain to source (that is, reverse) without activating the MX5015D22 Reverse Comparator. Higher $R_{DS(ON)}$ will reduce this reverse current level.
3. Cost. Generally, as the $R_{DS(ON)}$ rating goes lower, the cost of the MOSFET goes higher.
5. The dominate MOSFET loss for the MX5015D22 active OR-ing controller is conduction loss due to source-to- drain current to the output load, and the $R_{DS(ON)}$ of the MOSFET. This conduction loss could be reduced by using a MOSFET with the lowest possible $R_{DS(ON)}$. However, contrary to popular belief, arbitrarily selecting a MOSFET based solely on having low $R_{DS(ON)}$ may not always give desirable results for several reasons:

a. Selecting a MOSFET with an $R_{DS(ON)}$ that is too large will result in excessive power dissipation. Additionally, the MOSFET gate will be charged to the full value that the MX5015D22 can provide as it attempts to drive the Drain to Source voltage down to the $V_{SD(REG)}$ of 30mV typical. This increased Gate charge will require some finite amount of additional discharge time when the MOSFET needs to be turned off.

b. As a guideline, it is suggested that $R_{DS(ON)}$ be selected to provide at least 30mV, and no more than 100mV, at the nominal load current.

c. $(30mV / I_D) \leq R_{DS(ON)} \leq (100mV / I_D)$

d. The thermal resistance of the MOSFET package should also be considered against the anticipated dissipation in the MOSFET to ensure that the junction temperature (T_J) is reasonably well controlled, because the $R_{DS(ON)}$ of the MOSFET increases as the junction temperature increases.

6. $P_{DISS} = I_D^2 \times (R_{DS(ON)})$
7. Operating with a maximum ambient temperature ($T_{A(MAX)}$) of 35°C, a load current of 10 A, and an $R_{DS(ON)}$ of 10 mΩ, and desiring to keep the junction temperature under 100°C, the maximum junction-to-ambient thermal resistance rating (θ_{JA}) must be:

a. $R_{\theta JA} \leq (T_{J(MAX)} - T_{A(MAX)}) / (I_D^2 \times R_{DS(ON)})$

b. $R_{\theta JA} \leq (100°C - 35°C) / (10A \times 10A \times 0.01\Omega)$

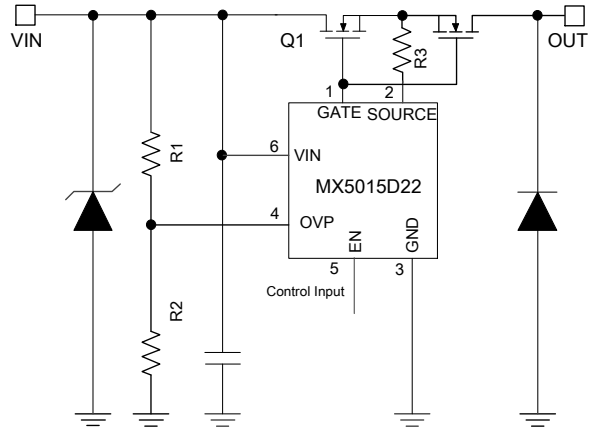
c. $R_{\theta JA} \leq 65°C/W$

Application guidelines

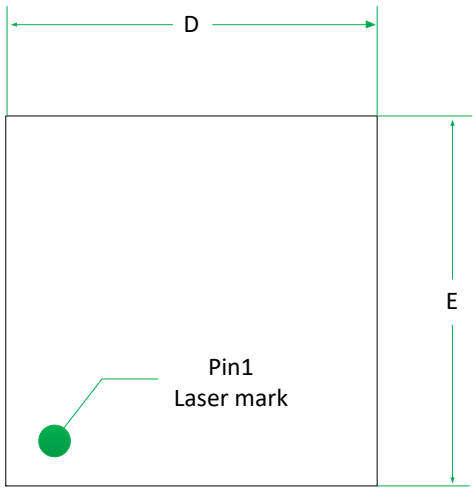
The layout of MX5015D22 is critical to its performance and functionality. The MX5015D22 is available in a 2x2 DFN, which allows a low inductance connection to a FET.

Place a TVS as close as to the input end prevent parasitic inductance oscillation from damaging the circuit. And a Schottky is placed at the output end to release oscillation caused by the output lead inductance. A 100~200ohm resistor

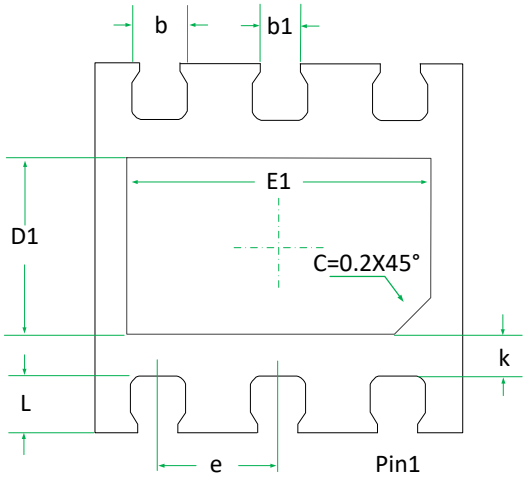
between the Source pin and output end to prevent damage from surge voltage, as the R3 shown in the figure below.



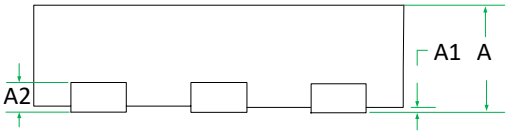
Package information



Top View



Bottom View

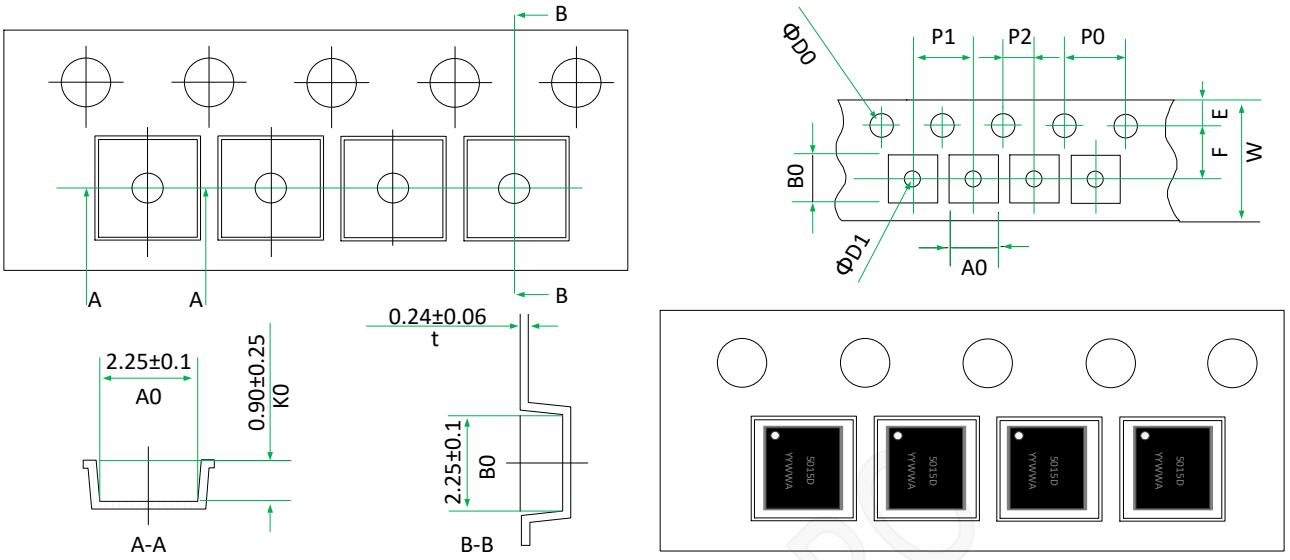


Side View

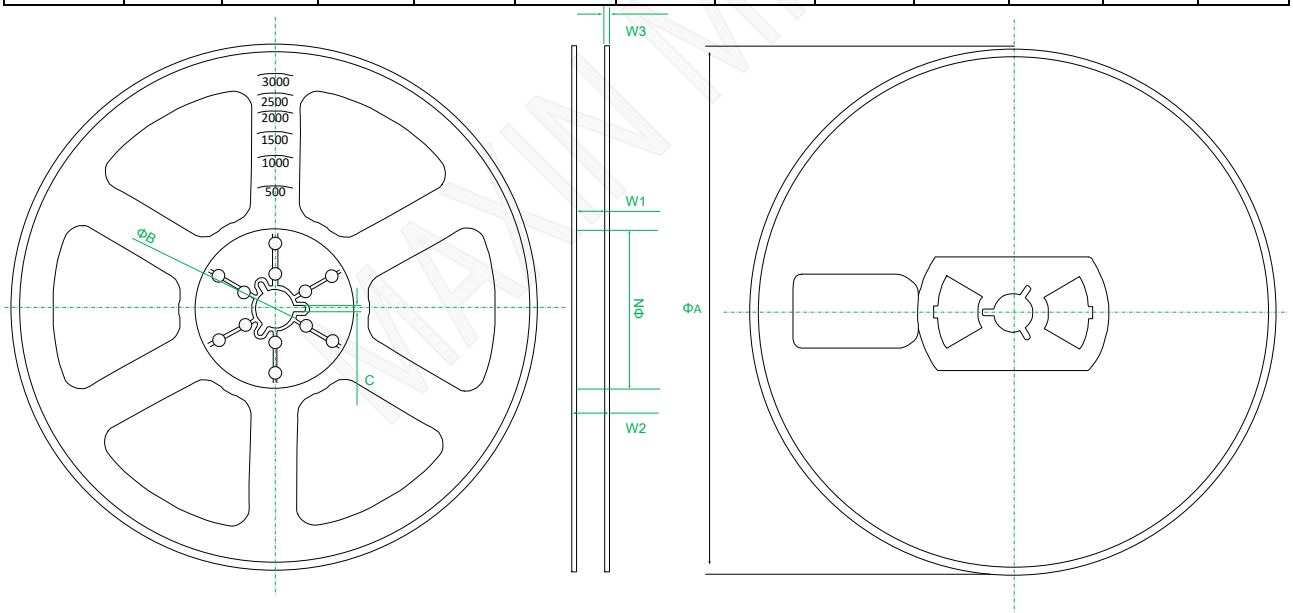
SYMBOL	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.50	0.55	0.60	0.02	0.022	0.024
A1	0	0.025	0.050	0	0.001	0.002
A2		0.152BSC			0.006BSC	
D	1.900	2.000	2.100	0.075	0.078	0.083
E	1.900	2.000	2.100	0.075	0.078	0.083
D1	0.860	0.960	1.060	0.034	0.038	0.042
E1	1.550	1.650	1.750	0.061	0.065	0.069
k		0.220BSC			0.008BSC	
b	0.250	0.300	0.350	0.010	0.012	0.014
b1		0.220BSC			0.008BSC	
e		0.650BSC			0.026BSC	
L	0.224	0.300	0.376	0.009	0.012	0.015

DFN2*2 for MX5015D22

Tape and Reel Information



Symbol	W	E	F	ΦD0	ΦD1	P0	P1	P2	A0	B0	K0	t
MAX	8.10	1.85	3.55	1.60	1.10	4.10	4.10	2.05	2.38	2.38	1.15	0.28
MIN	7.90	1.65	3.45	1.40	0.90	3.90	3.90	1.95	2.15	2.15	0.65	0.18



Symbol	ΦA	ΦN	ΦB	C	W1	W2	W3
MAX	180	56	13.5	2.50	9.9	12	1.8
MIN	176	52	13.0	1.90	8.4		1.0

Restrictions on Product Use

◆ MAXIN micro is continually working to improve the quality and reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing MAXIN products, to comply with the standards of safety in making a safe design for the entire system, and to avoid situations in which a malfunction or failure of such MAXIN products could cause loss of human life, bodily injury or damage to property.

◆ In developing your designs, please ensure that MAXIN products are used within specified operating ranges as set forth in the most recent MAXIN products specifications.

◆ The information contained herein is subject to change without notice.

Version update record:

V10 The original version （preliminary）