

GENERAL DESCRIPITION

MX1313AS is a secondary side switch IC designed for flyback converter. This IC emulate the behavior of diode rectifier for reduces power dissipation. MX1313AS works in DCM and quasi-resonant operation modes. Ruggedness and noise immunity are accomplished using an advanced blanking scheme and double pulse suppression which allow reliable operation in all operating modes.

MX1313AS senses the internal drain-source voltage, and output ideal drive signal with less external components. It only provides high performance solutions for 5V output voltage application.

MX1313AS is offered in SOP-8 package.

FEATURES

- ♦ Internal 40V 10mΩ trench MOSFET
- ◆ Up to 100kHz operation frequency
- ♦ 80ns turn on propagation delay and 50ns turn off delay
- ♦ Lower quiescent current consumption
- ◆ DCM and Quasi-resonant operation modes compatible
- ♦ VDD under voltage lock out

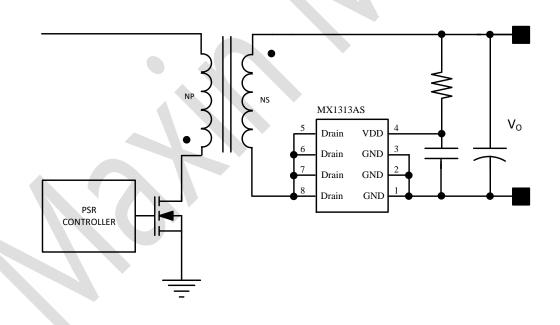
Applications

Cell Phone Charger

Auxiliary Power Adapter

Digital Cameras Charger

Typical Application





Synchronous Rectifier for Flyback DCM and QR Converter

General information

Ordering information

Part Number	Description
MX1313AS	SOP8, Halogen-free, RoHS

Package dissipation rating

Package	RθJA (°C/W)
SOP8	90

Note: Drain Pin Connected to 200mm² PCB copper clad.

Absolute maximum ratings

Parameter	Value
Drain Voltage (off state)	40
VDD Voltage	-0.3 to 7V
Min/Max Operating Junction	-40 to 150°C
Temperature TJ	-40 to 130 C
Min/Max Storage Temperature	-55 to 150°C
Tstg	-33 to 130 C
ESD(HBM)	±2kV
Lead Temperature (Soldering,	260℃
10secs)	200 C

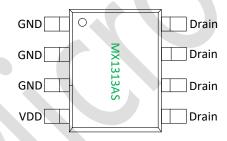
Note: stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Marking information

Recommended operating condition

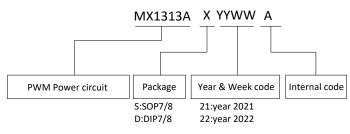
Symbol	Parameter	Range
VDD	VDD supply voltage	3.5-
		5.5V
PD	Power dissipation @TA=25℃	1.1W
Output	5V3.1A typical	15.5W
power		

Terminal assignments



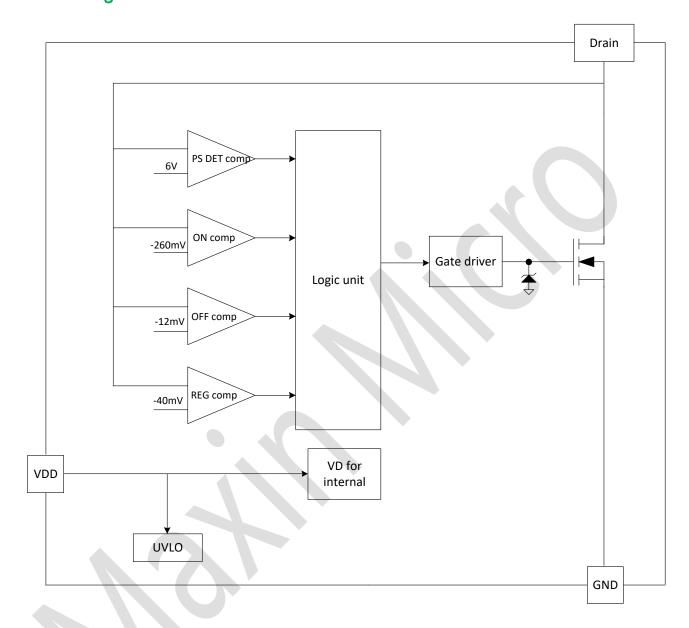
PIN	PIN	Description			
NO.	name				
1/2/3 GND		Power ground, the source of internal			
1/2/3	GND	MOSFET.			
4	VDD	Power supply.			
5/6/7/8	Drain	Internal MOSFET drain side.			







Block Diagram





Electrical characteristics

(TA=25 $^{\circ}$ C , VDD=5V, unless otherwise noted)

Symbol	Parameter	Test condition	Min	Тур.	Max	Unit	
VDD supply voltage							
I_VDD	Quiescent current	VDD=5.5V	200	300	500	μΑ	
UVLO_ON	VDD under voltage lockout enter	VDD rising up	2.3	2.5	2.8	V	
UVLO_OFF	VDD under voltage lockout exit		2.6	2.8	3.1	V	
Control circui	try section						
V _{ON_TH}	Turn on threshold (V _{DRAIN} -V _{SOURCE})		300	260	-200	mV	
Ton_delay	Turn on propagation delay			80		ns	
V _{OFF_TH}	Turn off threshold (Vsource-Vdrain)		-20	-12	-9	mV	
Toff_delay	Turn off propagation delay			50		ns	
V _{REG(DRV)}	Drive regulation voltage		-50	-40	-32	mV	
Ton_min	Minimum on time		500	600	900	ns	
Toff_min	Minimum off time		1.3	1.6	2.4	μs	
VPS_ON_DET	Primary side on detection voltage			6		V	
TPS_ON_DET	Primary side on detection blanking time			300		ns	
MOSFET							
RDS_ON	Static Drain to Source on resistance			10		mΩ	
VDS	Drain to Source breakdown voltage		40			V	



Synchronous Rectifier for Flyback DCM and QR Converter

Operation description

MX1313AS detects the drain to source voltage of internal MOSFET. When the secondary winding is on, the current flow the parasitic diode of MOSFET. If the drain voltage is lower than the turn on threshold voltage $V_{\rm ON_TH}$, the internal drive circuit turn on the MOSFET after a turn on delay time $T_{\rm ON\ DELAY}$. Then the lower conduction loss can be achieved.

UVLO and Power Supply

MX1313AS remains in the UVLO condition until the voltage on the VDD exceeds the voltage UVLO_ON. During the time the gate drive circuit is inactive. The UVLO mode is accessible from any other state of operation whenever MX1313AS supply voltage condition of VDD is smaller than UVLO_OFF occurs.

MX1313AS supply voltage is monitored by the UVLO circuit. It is possible to turn off the circuit by pulling VDD voltage below the turn off threshold voltage. To prevent noise problems, a bypass ceramic capacitor connected to VDD and GND.

Minimum ON time

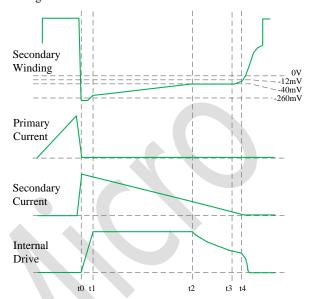
When the internal MOSFET is turned on and some ringing noise may be generated. If that noise falls below the threshold VOFF_TH before minimum on time expires, the internal MOSFET will keep on until the end of the minimum on time.

Turn On and Turn OFF Phase

When second winding is on, current will start flowing through its body diode, generating a negative voltage between drain and source. When the voltage up to the turn on threshold $V_{\rm TH_ON}$, internal circuit will drive the gate of internal MOSFET on, which will in turn cause the conduction voltage to drop down. The minimum on time will prevent the turn off from some amount of ringing. And the Drain to Source voltage will shrink as the secondary current decreases. Then the Drian to Source voltage will be maintained -40mV by adjusting internal drive voltage.

When the current flowing close to 0A, the -40mV will not be maintained by internal driver. The Drain to Source voltage continue rising which to reach the threshold V_{OFF_TH} (-12mV typical), the internal MOSFET will be turned off after the propagation delay time T_{OFF_DELAY}. After the internal MOSFET is turned off, it is necessary to detect that the Drian to Source voltage reach about 6V or more and after a

continuation time greater than T_{PS_ON_DET} (300ns typical), a valid primary side turn on is confirmed to avoid false turn on caused by quasi-resonant. The following figure shows the timing of turn on and turn off.



The timing of turn on and turn off

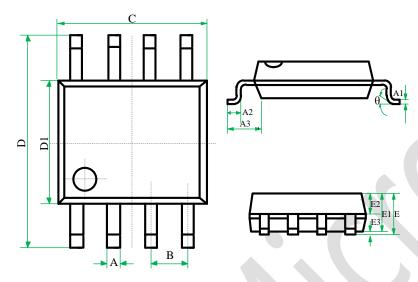
Minimum ON time

The aera of the secondary current loop including the MX1313AS and the output capacitor should be as small as possible to reduce EMI radiation. And the PCB trace must be wide and short for thermal consideration.

The bypass capacitor on VDD should be placed as close as possible to the VDD pin. And the negative node of VDD capacitor should be connected directly to the GND pin.



Package information



CVMDOI	MILLIMETERS			INCHES		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	0.39	-	0.48	0.0154	-	0.0189
A1	0.21	-	0.28	0.008	-	0.011
A2	0.50	-	0.80	0.020	-	0.031
A3	1.05BSC			1.05BSC 0.041BSC		
В	1.27BSC			0.050BSC		
С	4.70	4.90	5.10	0.185	0.193	0.201
D	5.80	6.00	6.20	0.228	0.236	0.244
D1	3.70	3.90	4.10	0.146	0.154	0.161
Е	-	-	1.75	-	-	0.069
E1	1.30	1.40	1.50	0.051	0.055	0.059
E2	0.60	0.65	0.70	0.024	0.026	0.028
E3	0.10	-	0.225	0.004	-	0.009
θ	0	-	8°	0	-	8°

SOP8 for MX1313AS

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