

GENERAL DESCRIPITION

MX1217E6 is a high-performance current mode PWM power circuit, it combines a dedicated PWM controller with a high voltage power MOSFET. It is optimized for high performance, low standby power, and cost effective off-line flyback converter applications.

MX1217E6 offers comprehensive protection coverage with auto-recovery including Cycle-by-Cycle current limiting (OCP), over load protection (OLP), Output diode short circuit protection, VDD under voltage lockout (UVLO), internal over temperature protection (OTP). Excellent EMI performance is achieved with MAXIN proprietary frequency shuffling technique.

The tone energy at below 22KHz is minimized in the design and audio noise is eliminated during operation.

MX1217E6 is offered in ESOP-6L package.

Applications

Offline AC/DC flyback converter

PD charger

Wide output range adapter

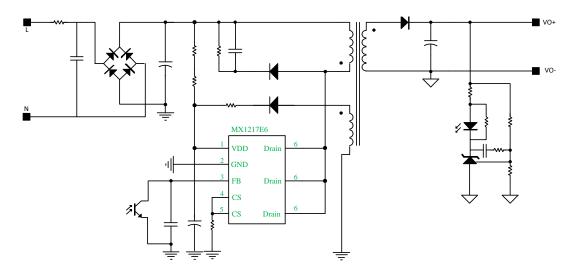
FEATURES

- ◆ Low VDD startup current and low operating current
- ♦ Very wide range of VDD supply voltage
- ◆ Standby power < 75mW
- ◆ Power on soft start reducing MOSFET VDS stress
- ◆ Frequency shuffling for EMI
- Extended burst mode control for improved efficiency and minimum standby power design
- ♦ Fixed 65KHZ (typical) switching frequency
- ♦ Internal synchronized slope compensation
- ♦ Leading edge blanking on current sense input
- ◆ Comprehensive protection coverage
 - VDD Under Voltage Lockout with hysteresis (UVLO)
 - VDD Over Voltage Protection (VDD OVP)
 - Cycle-by-cycle over current protection
 - Over Load Protection (OLP) with auto-recovery
 - Output diode short protection with auto-recovery

Recommended operating condition

Symbol	Parameter	Range
VDD	VDD supply voltage	9-48V
PD	Power dissipation @TA=25℃	1.5W
Output power	Open frame	30W

Typical Application





General information

Ordering information

Part Number	Description
MX1217E6	ESOP-6L, Halogen-free, RoHS

Package dissipation rating

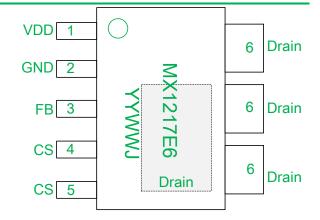
Package	RθJA (°C/W)
ESOP-6L	65

Note: Drain Pin Connected to 200mm2 PCB copper clad.

Absolute maximum ratings

Parameter	Value
Drain Voltage (off state)	650
VDD Voltage	60 V
FB Input Voltage	-0.3 to 7V
CS Input Voltage	-0.3 to 7V
Min/Max Operating Junction	-40 to 150℃
Temperature TJ	
Min/Max Storage Temperature T _{STG}	-55 to 150℃
Lead Temperature (Soldering,	260℃
10secs)	

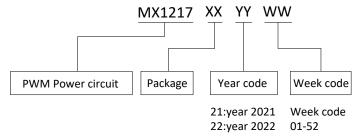
Note: stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.



PIN	PIN	Description				
NO.	name	1				
1	VDD	Power supply.				
2	GND	Ground pin.				
3	FB	Feedback input pin. The PWM duty cycle is determined by voltage level into this pin and current-sense signal CS pin.				
4、5	CS	Current sense pin, connect resistors to ground external for cycle-by-cycle current limiting.				
6、 PAD	Drain	The Drain of the internal power MOSFET, connect the primary winding of transformer.				

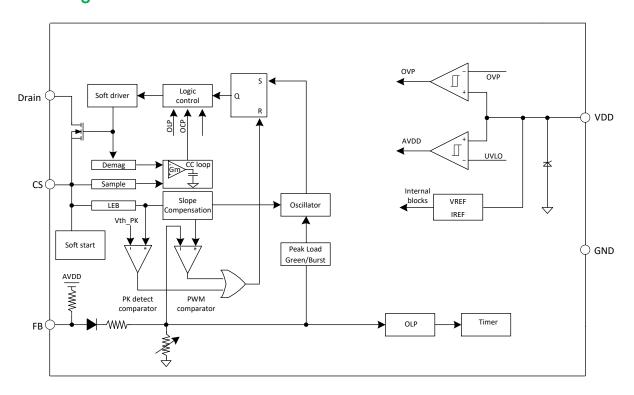
Terminal assignments







Block Diagram





Electrical characteristics

(TA=25°C, VDD=18V, unless otherwise noted)

INDITECT VDD startup (VDD startup current) VDD—INVECTOR 1.0 2.0 5.0 μ LyDD VDD normal operation current VDD—INV, CS=0V, FB=-5.5V 2.0 3.0 m LyDD Burst mode operation current VDD—INV, CS=0V, FB=-0.5V 0.5 m UVLO_ONF VDD under voltage lockout enter CS=3.3V. VDD step down 6.7 7.2 7.7 V UVLO_OPF VDD under voltage lockout exit CS=3.3V. VDD step up 15.0 16.5 17.0 V VDD_10VP Over voltage protection voltage FB=3V, CS=0V. VDD step up 50.0 52.0 54.0 V V_Latch Latch release voltage External OTP/VDD_OVP/VO_OVP 6.0 4.8 8.0 V V_Latch Latch release voltage External OTP/VDD_OVP/VO_OVP 6.0 5.1 4.0 V V_Latch Latch release voltage External OTP/VDD_OVP/VD_OVP 7.0 5.1 V V_Latch Latch Latch 1.0 1.0 V <t< th=""><th>Symbol</th><th colspan="2">Parameter Test condition</th><th>Min</th><th>Тур.</th><th>Max</th><th>Unit</th></t<>	Symbol	Parameter Test condition		Min	Тур.	Max	Unit
I. VDD	VDD supply vo	oltage					
Burst Burst Burst Burst Mode operation current CS=3.3V, VDD step down 6.7 7.2 7.7 V VUVLO_OFF VDD under voltage lockout enter CS=3.3V, VDD step down 6.7 7.2 7.7 V VUVLO_OFF VDD under voltage lockout exit CS=3.3V, VDD step up 15.5 16.5 17.5 V VDD_OVP Vover voltage protection voltage FB=3V, CS=0V, VDD step up 50.0 52.0 54.0 V V_Latch Latch release voltage External OTP/ VDD_OVP/VO_OVP 4.8 V V_Latch Latch release voltage External OTP/ VDD_OVP/VO_OVP 4.8 V V_Latch Latch release voltage External OTP/ VDD_OVP/VO_OVP 4.8 V V_LATCH Latch release voltage External OTP/ VDD_OVP/VO_OVP 4.8 V V_LATCH V_LAT	I startup	VDD startup current	VDD=UVLO_OFF-1V		2.0	5.0	μΑ
UVLO_ON VDD under voltage lockout enter CS=3.3V. VDD step up 6.7 7.2 7.7 V UVLO_OFF VDD under voltage lockout exit CS=3.3V. VDD step up 15.5 16.5 17.5 V VDD_OVP Over voltage protection voltage Esternal OTP/ VDD_OVP/ VO_OVP 4.8 V V_Latch Latch release voltage Esternal OTP/ VDD_OVP/ VO_OVP 4.8 V T_recovery Restart time for auto-recovery protection Esternal OTP/ VDD_OVP/ VO_OVP 4.8 V V_Latch Restart time for auto-recovery protection Esternal OTP/ VDD_OVP/ VO_OVP 4.8 V V_Encent Restart time for auto-recovery protection To the step of the protection of auto-recovery protection To the step of auto-recovery protection To the step of auto-recovery protection To V PB_Bins PB Open Boop voltage PD_IAN CAPP To UN To V V	I_VDD	VDD normal operation current	VDD=18V, CS=0V, FB=2.5V		2	3	mA
UVLO_OFF VDD under voltage lockout exit CS=3.3V. VDD step up 15.5 16.5 17.5 V VDD_OVP Over voltage protection voltage FB=3V. CS=0V. VDD step up 50.0 52.0 54.0 V V_Latch Lach release voltage External OTP/VDD_OVP/VO_OVP 4.8 7.0 V T_cecovery Restart time for auto-recovery protection Total Call Call Call Call Call Call Call C	I_ Burst	Burst mode operation current	VDD=18V, CS=0V, FB=0.5V		0.3	0.5	mA
VDD_OVP Over voltage protection voltage FB=3V, CS=0V, VDD step up 50.0 52.0 54.0 V V_Latch Latch release voltage External OTP/VDD_OVP/VO_OVP 4.8 1.0 V V_Latch Latch release voltage External OTP/VDD_OVP/VO_OVP 4.8 1.0 V T_recovery Restart time for autor-recovery protection 5.1 1.0 x s FB pin Feedback stratt time for autor-recovery protection VDD_TBMAX FB pin floor voltage 5.1 V V V VDD_TBMAY Max duty eyele VDD=18V, VFB=3V, VCS=0.3V 70 90 % Max duty eyele VDD=18V, VFB=3V, VCS=0.3V 70 2.05 % Max duty eyele VDD=18V, VFB=3V, VCS=0.3V 70 2.05 % Max duty eyele VDD=18V, VFB=3V, VCS=0.3V 70 2.05 % Max duty eyele VDD=18V, VFB=3V, VCS=0.3V 70 2.05 % VVRBTB_about 1.1 1.2 V VVRBTB_about 1.1 1.2 1.0 VVRBTB_about 1.1 1.2 V VVRBTB_about 1.1	UVLO_ON	VDD under voltage lockout enter	CS=3.3V, VDD step down	6.7	7.2	7.7	V
V_Latch Latch release voltage External OTP/ VDD_OVP/ VO_OVP 4.8 V T_recovery Restart time for auto-recovery protection Latch 1.4 Latch S FB pin - Feedbase kinput section VFB_Opsa FB Open loop voltage S.1 S.1 V Aves PWM input gain ΔYFB/ΔVCS 3.3 3.3 V/V D_MAX Max duty cycle VDD=18V, VFB=3V, VCS=0.3V 70 90 % IFB_short The threshold enters green mode VDD=18V, CS=0V, FB step down 2.05 2.0 mA V PRE_Bens_H The threshold enters burst mode VDD=18V, CS=0V, FB step down 1.1 1.2 V V PRE_Bens_L The threshold enters burst mode VDD=18V, CS=0V, FB step down 1.1 1.2 V V PRE_Bens_L The threshold enters burst mode VDD=18V, CS=0V, FB step down 1.1 1.2 V V PRE_Bens_L The threshold enters burst mode VDD=18V, CS=0V, FB step down 1.1 1.0 W T D_OLD Open loop protection threshold 4.0	UVLO_OFF	VDD under voltage lockout exit	CS=3.3V, VDD step up	15.5	16.5	17.5	V
T_recovery Restart time for auto-recovery protection FB pin - Feedback input section	VDD_OVP	Over voltage protection voltage	FB=3V, CS=0V, VDD step up	50.0	52.0	54.0	V
FB pin - Feedback input section VFB_Open FB open loop voltage	V_Latch	Latch release voltage	External OTP/ VDD_OVP/ VO_OVP		4.8		V
VFIL Open FB open loop voltage	T_recovery	Restart time for auto-recovery protection			1.4		s
No. No.	FB pin – Feedb	pack input section					
D_MAX Max duty cycle VDD=18V, VFB=3V, VCS=0.3V 70 % 90 % IFB_short FB pin short circuit current Current for short FB to GND 0.25 1 mA VFB_green The threshold enters green mode VDD=18V, CS=0V, FB step down 2.05 2 V VREF_burst_L The threshold exits burst mode VDD=18V, CS=0V, FB step up 1.1 2 V VREF_burst_L The threshold enters burst mode VDD=18V, CS=0V, FB step down 1.1 4.0 4.4 4.8 V VTI_OLP Over load protection threshold 4.0 4.4 4.8 V TD_OLP Open loop protection debounce time 6 60 ms ms RFB_IN FB input impedance 8 4.0 4.0 4.0 ms CS pin—Current FB input impedance 9 4.0 4.0 ms T_D.OC Soft start time of CS threshold 1 4.0 4.0 ms T_D.OC Over current detection and delay From over current occurs till gate dr	V _{FB_Open}	FB open loop voltage			5.1		V
If B _D , short FB pin short circuit current Current for short FB to GND 0.25 m Manal VFB_green The threshold enters green mode VDD=18V, CS=0V, FB step down 2.05 V VREF_bunst_H The threshold exits burst mode VDD=18V, CS=0V, FB step upp 1.2 V VREF_bunst_L The threshold enters burst mode VDD=18V, CS=0V, FB step down 1.1 V VTH_OLP Over load protection threshold 4.0 4.4 4.8 V TD_OLP Open loop protection debounce time 60 4.0 4.0 4.0 Mrs RFB_IN FB input impedance	Avcs	PWM input gain ΔVFB/ΔVCS			3.3		V/V
The threshold enters green mode VDD=18V, CS=0V, FB step down L2 V VREF_burst_H The threshold exits burst mode VDD=18V, CS=0V, FB step up L2 V VREF_burst_L The threshold exits burst mode VDD=18V, CS=0V, FB step down L1 L2 V VREF_burst_L The threshold enters burst mode VDD=18V, CS=0V, FB step down L1 L1 V VREF_burst_L The threshold enters burst mode VDD=18V, CS=0V, FB step down L1 L1 V VREF_burst_L The threshold enters burst mode VDD=18V, CS=0V, FB step down L1 L1 L1 V VREF_burst_L The threshold enters burst mode VDD=18V, CS=0V, FB step down L1 L1 L1 L1 L2 R The threshold enters burst mode VDD=18V, CS=0V, FB step down L1 L1 L1 L1 R The threshold enters burst mode VDD=18V, CS=0V, FB step down L1 L1 L1 R The threshold enters burst mode VDD=18V, CS=0V, FB step down L1 L1 L1 The threshold enters burst mode VDD=18V, CS=0V, FB step up L1 L1 L1 The threshold enters burst mode VDD=18V, CS=0V, FB step up L1 L1 L1 The threshold enters burst mode VDD=18V, CS=0V, FB step up L1 L1 L1 The threshold enters burst mode VDD=18V, CS=0V, FB step up L1 L1 The threshold enters burst mode VDD=18V, FB=2.5V The threshold enters burst mode VDD=18V, FB=2.5V The threshold enters burst mode VDD=18V, FB=2.5V The threshold enters burst mode The threshold enters burst mo	D_MAX	Max duty cycle	VDD=18V, VFB=3V, VCS=0.3V	70		90	%
VREE_burst_H The threshold exits burst mode VDD=18V, CS=0V, FB step up 1.2 V VREE_burst_L The threshold enters burst mode VDD=18V, CS=0V, FB step down 1.1 V VTH_OLP Over load protection threshold 4.0 4.4 4.8 V TD_OLP Open loop protection debounce time 60 ms ms RFB_IN FB input impedance 50 kQ kQ CS pin - Current FB input impedance 50 4.0 ms TCS_pin - Current FS input impedance 50 4.0 ms T_S_SST Soft start time of CS threshold 4.0 ms ms T_blanking Leading edge blanking time 300 1 ns T_D_OC Over current detection and delay From over current occurs till gate driver turns off 0.492 0.500 0.508 V VCS_PK_clamp CS voltage clamper 0.492 0.500 0.508 V VCS_PK_clamp CS voltage clamper 1.1 1.2 1.3 V	I _{FB_short}	FB pin short circuit current	Current for short FB to GND		0.25		mA
VREF_burs_L The threshold enters burst mode VDD=18V, CS=0V, FB step down 1.1 V VTH_OLP Over load protection threshold 4.0 4.4 4.8 V TD_OLP Open loop protection debounce time 60 ms RFB_IN FB input impedance 20 kΩ CS pin - Current sense input To_S_SST Soft start time of CS threshold 4.0 ms T_blanking Leading edge blanking time 300 ns T_D_OC Over current detection and delay From over current occurs till gate driver turns off 90 ns VCS_PK Internal current limiting threshold voltage with zero duty cycle 0.492 0.500 0.508 V VCS_PK_Clamp CS voltage clamper 0.715 V V VCS_PK_Clamp Second rectifier diode short protection threshold voltage 1.1 1.2 1.3 V Oscillator Frequency jittering 7 47 % Fosc_sbuffling Shuffling frequency 40 Hz Fosc_tbuffling Frequency temperature stability 1.0 65 Hz </td <td>V_{FB_green}</td> <td>The threshold enters green mode</td> <td>VDD=18V, CS=0V, FB step down</td> <td></td> <td>2.05</td> <td></td> <td>V</td>	V _{FB_green}	The threshold enters green mode	VDD=18V, CS=0V, FB step down		2.05		V
VTH_OLP Over load protection threshold 4.0 4.4 4.8 V T_{DOLP} Open loop protection debounce time 60 ms R_{FBLN} FB input impedance 20 kΩ CS pin – Current sense input Tos_sst Soft start time of CS threshold 4.0 ms T_Dlanking Leading edge blanking time 300 ns T_D_oc Over current detection and delay From over current occurs till gate driver turns off 90 ns V_{CS_PK} Internal current limiting threshold voltage with zero duty cycle 0.492 0.500 0.508 V V_{CS_PK_clamp} CS voltage clamper 0.715 V V V_{CS_SRST} Second rectifier diode short protection threshold voltage 1.1 1.2 1.3 V Osc_NOM Normal frequency of high output voltage VDD=18V, FB=2.5V 65 kHz Fosc_shuffling Shuffling frequency -7 -7 +7 % Fosc_stantfling Frequency temperatur	V _{REF_burst_H}	The threshold exits burst mode	VDD=18V, CS=0V, FB step up		1.2		V
TD_OLP Open loop protection debounce time 60 ms	V _{REF_burst_L}	The threshold enters burst mode	VDD=18V, CS=0V, FB step down		1.1		V
RFB_IN FB input impedance 20 kΩ CS pin – Current sense input TCS_SST Soft start time of CS threshold 4.0 ms T_blanking Leading edge blanking time 300 ns T_b_oc Over current detection and delay From over current occurs till gate driver turns off 90 ns VCS_PK Internal current limiting threshold voltage with zero duty cycle 0.492 0.500 0.508 V VCS_PKclamp CS voltage clamper 0.715 0.715 V V VCS_SRST Second rectifier diode short protection threshold voltage 1.1 1.2 1.3 V Oscillator Fosc_NoM Normal frequency of high output voltage VDD=18V, FB=2.5V 65 kHz Fosc_TEMP Frequency jittering -7 -7 +7 % Fosc_TEMP Frequency temperature stability 1.0 % 65 L Hz Fosc_VDD Frequency VDD voltage stability 1.0 1.0 % 1.0 %	V _{TH_OLP}	Over load protection threshold		4.0	4.4	4.8	V
CS pin – Current sense input Tcs_sst Soft start time of CS threshold 4.0 ms T_blanking Leading edge blanking time 300 ns Tb_oc Over current detection and delay From over current occurs till gate driver turns off 90 ns Vcs_PK Internal current limiting threshold voltage with zero duty cycle 0.492 0.500 0.508 V Vcs_PKclamp CS voltage clamper 0.715 0.715 V Vcs_SRST Second rectifier diode short protection threshold voltage 1.1 1.2 1.3 V Oscillator Fosc_NOM Normal frequency of high output voltage VDD=18V, FB=2.5V 65 kHz Fosc_JT Frequency jittering -7 +7 +7 % Fosc_TEMP Frequency temperature stability 1.0 % Fosc_VDD Frequency VDD voltage stability 1.0 %	T _{D_OLP}	Open loop protection debounce time			60		ms
TCS_SST Soft start time of CS threshold 4.0 ms T_blanking Leading edge blanking time 300 ns TD_OC Over current detection and delay From over current occurs till gate driver turns off 90 ln ns VCS_PK Internal current limiting threshold voltage with zero duty cycle 0.492 0.500 0.508 V VCS_PKclamp CS voltage clamper 0.715 0.715 V VCS_SRST Second rectifier diode short protection threshold voltage 1.1 1.2 1.3 V Oscillator Fosc_NOM Normal frequency of high output voltage VDD=18V, FB=2.5V 65 kHz Fosc_JT Frequency jittering -7 -7 +7 % Fosc_sbuffling Shuffling frequency -240 Hz Fosc_telmp Frequency temperature stability 1.0 % Fosc_vdd Frequency VDD voltage stability 1.0 %	R _{FB_IN}	FB input impedance			20		kΩ
T_blanking	CS pin – Curre	nt sense input					
TD_OC Over current detection and delay From over current occurs till gate driver turns off VCS_PK Internal current limiting threshold voltage with zero duty cycle CS voltage clamper CS voltage clamper Second rectifier diode short protection threshold voltage Nosc_INGM Normal frequency of high output voltage Fosc_NOM Normal frequency of high output voltage VDD=18V, FB=2.5V Fosc_JT Frequency jittering Shuffling frequency Fosc_TEMP Frequency temperature stability Fosc_TEMP Frequency VDD voltage stability From over current occurs till gate driver turns off Prom over current occurs till gate driver turns off Prom over current occurs till gate driver turns off Posc_NOM Posc_S_NOM Note and in threshold voltage From over current occurs till gate driver turns off Posc_NOM Posc_S_NOM Note and in threshold voltage Prom over current occurs till gate driver turns off Posc_NOM Posc_S_NOM Posc_S_NOM Posc_S_NOM Normal frequency of high output voltage VDD=18V, FB=2.5V Posc_SE_ST Prequency jittering Prequency jittering Prequency temperature stability Prosc_TEMP Frequency VDD voltage stability Prom over current occurs till gate driver turns off Posc_NOM Posc_S_NOM Posc_SE_ST Prom over current occurs till gate driver turns off Posc_NOM Posc_S_NOM Posc_S_NOM Posc_S_NOM Posc_SE_SE_ST Posc_SE_SE_SE_S_S_S_S_S_S_S_S_S_S_S_S_S_S_S	Tcs_sst	Soft start time of CS threshold			4.0		ms
TD_OC Over current detection and delay driver turns off 90 ns VCS_PK Internal current limiting threshold voltage with zero duty cycle 0.492 0.500 0.508 V VCS_PKclamp CS voltage clamper 0.715 V VCS_SRST Second rectifier diode short protection threshold voltage 1.1 1.2 1.3 V Oscillator FOSC_NOM Normal frequency of high output voltage VDD=18V, FB=2.5V 65 kHz FOSC_ST Frequency jittering 7.7 +7 % FOSC_Shuffling Shuffling frequency 6 Hz FOSC_TEMP Frequency temperature stability 1.0 % Fosc_VDD Frequency VDD voltage stability 1.0 %	T_blanking	Leading edge blanking time			300		ns
VCS_PK Internal current limiting threshold voltage with zero duty cycle 0.492 0.500 0.508 V VCS_PKclamp CS voltage clamper 0.715 V VCS_SRST Second rectifier diode short protection threshold voltage 1.1 1.2 1.3 V Oscillator Fosc_NOM Normal frequency of high output voltage VDD=18V, FB=2.5V 65 kHz Fosc_JT Frequency jittering -7 +7 % Fosc_shuffling Shuffling frequency 240 Hz Fosc_TEMP Frequency temperature stability 1.0 % Fosc_VDD Frequency VDD voltage stability 1.0 %	T _{D_OC}	Over current detection and delay	_		90		ns
VCS_PK with zero duty cycle 0.492 0.500 0.508 V VCS_PKclamp CS voltage clamper 0.715 V VCS_SRST Second rectifier diode short protection threshold voltage 1.1 1.2 1.3 V Oscillator FOSC_NOM Normal frequency of high output voltage VDD=18V, FB=2.5V 65 kHz FOSC_JT Frequency jittering -7 +7 % FOSC_shuffling Shuffling frequency 240 Hz FOSC_TEMP Frequency temperature stability 1.0 % Fosc_VDD Frequency VDD voltage stability 1.0 %			driver turns off				
VCS_PKclamp CS voltage clamper 0.715 V VCS_SRST Second rectifier diode short protection threshold voltage 1.1 1.2 1.3 V Oscillator FOSC_NOM Normal frequency of high output voltage VDD=18V, FB=2.5V 65 kHz FOSC_JT Frequency jittering -7 +7 % FOSC_shuffling Shuffling frequency 240 Hz FOSC_TEMP Frequency temperature stability 1.0 % Fosc_VDD Frequency VDD voltage stability 1.0 %	V _{CS_PK}			0.492	0.500	0.508	V
VCS_SRST Second rectifier diode short protection threshold voltage Oscillator Fosc_Nom Normal frequency of high output voltage VDD=18V, FB=2.5V 65 kHz Fosc_Struffling Frequency jittering -7 +7 % Fosc_shuffling Shuffling frequency Fosc_TEMP Frequency temperature stability Fosc_VDD Frequency VDD voltage stability 1.0 %	V				0.715		3 7
Vcs_srst threshold voltage 1.1 1.2 1.3 V Oscillator Fosc_Nom Normal frequency of high output voltage VDD=18V, FB=2.5V 65 kHz Fosc_JT Frequency jittering -7 +7 % Fosc_shuffling Shuffling frequency 240 Hz Fosc_TEMP Frequency temperature stability 1.0 % Fosc_VDD Frequency VDD voltage stability 1.0 %	V CS_PKclamp	*			0.713		v
FOSC_NOM Normal frequency of high output voltage VDD=18V, FB=2.5V 65 kHz FOSC_JT Frequency jittering -7 +7 % FOSC_shuffling Shuffling frequency 240 Hz FOSC_TEMP Frequency temperature stability 1.0 % FOSC_VDD Frequency VDD voltage stability 1.0 %	V _{CS_SRST}			1.1	1.2	1.3	V
Fosc_shuffling Frequency jittering -7 +7 % Fosc_shuffling Shuffling frequency 240 Hz Fosc_TEMP Frequency temperature stability 1.0 % Fosc_VDD Frequency VDD voltage stability 1.0 %	Oscillator						
FOSC_Shuffling Shuffling frequency 240 Hz FOSC_TEMP Frequency temperature stability 1.0 % FOSC_VDD Frequency VDD voltage stability 1.0 %	F _{OSC_NOM}	Normal frequency of high output voltage	VDD=18V, FB=2.5V		65		kHz
FOSC_TEMP Frequency temperature stability 1.0 % FOSC_VDD Frequency VDD voltage stability 1.0 %	F _{OSC_JT}	Frequency jittering		-7		+7	%
Fosc_vdd Frequency VDD voltage stability 1.0 %	Fosc_shuffling	Shuffling frequency			240		Hz
	Fosc_temp	Frequency temperature stability			1.0		%
Fosc_burst Burst mode frequency 22 kHz	Fosc_vdd	Frequency VDD voltage stability			1.0		%
	Fosc_burst	Burst mode frequency			22		kHz



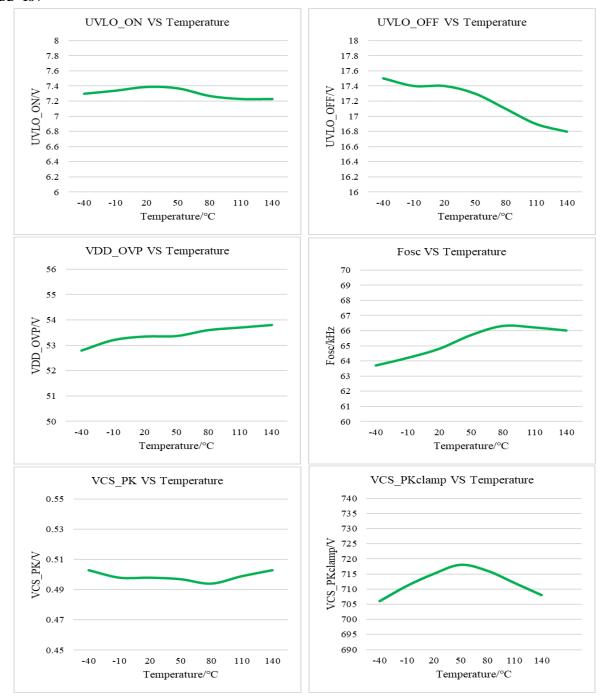
High Performance Current Mode PWM Power Circuit

GATE Driver						
V_{GL}	Gate low voltage	VDD=18V, Io=20mA			1.0	V
V_{GH}	Gate high voltage	VDD=18V, Io=20mA	8.0			V
V _{G_clamping}	Gate clamp voltage	VDD=18V		11.5		V
T_rise	Gate voltage rising time	1.2V ~ 10.8V @ CL=1000pF		140		ns
T_fall	Gate voltage falling time	10.8V ~ 1.2V @ CL=1000pF		55		ns
MOSFET						
RDS_ON	Static Drain to Source on resistance			1.2		Ω
VDS	Drain to Source breakdown voltage		650			V
Internal OTP						
OTP_in				150		$^{\circ}$
OTP_out				120		$^{\circ}$ C



Characteristic plots

VDD=18V





Operation description

MX1217E6 is a high-performance current mode PWM power circuit for low standby power and cost-effective charger and adapter applications. MX1217E6 is combined a high voltage power MOSFET and current mode PWM control IC. The 'extended burst mode' control greatly reduces the standby power consumption and helps the design easier to meet the international power conservation requirements.

Startup current and operation current

The VDD voltage of MX1217E6 could be charged up to UVLO_OFF threshold level and device starts up quickly as the startup current is designed to be very low. A large value startup resistor can therefore be used to minimize the power loss yet achieve a reliable startup in application.

To optimize power efficiency, startup resistors can be added to the AC line, which not only can reduce power loss but can reset latched mode protections faster.

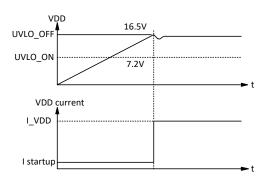


Fig1 startup current timing

The typical operating current of MX1217E6 is 2mA (typical). Good efficiency is achieved with this low operating current together with the extended burst mode control features.

Soft start

MX1217E6 features an internal 4.0ms(typical) soft start to soften the electrical stress occurring in the power supply during startup. It is activated during the power in sequence. As soon as VDD reaches UVLO_OFF, the CS peak voltage is gradually increased from 0.05V to the maximum level. Every restart up begins with a soft start.

Frequency shuffling for EMI improvement

The frequency shuffling is implemented in MX1217E6. The oscillation frequency is modulated so that the tone energy is

spread out. The spread spectrum minimizes the system design.

Extended burst mode operation

At light load or no-load condition, most of the power dissipation in a switching mode power supply is from switching loss of the MOSFET, the core loss of the transformer and the loss of the snubber circuit. The magnitude of power loss is in proportion to the switching frequency. Lower switching frequency leads to the reduction on the power loss and thus conserves the energy.

The switching frequency is internally adjusted at light load or no-load condition. The switching frequency reduces at light load or no load to improve the conversion efficiency. At light load or no-load condition, the FB input drops below VREF_burst_L and system enters burst mode. The gate drive output switches when FB input rise back to VREF_burst_H. Otherwise the gate drive remains at off state to minimize the switching loss and reduces the standby power consumption to the greatest extend.

The switching frequency control also eliminates the audio noise at any loading conditions.

Oscillator operation

During the full load power operation, MX1210 operates at 65kHz fixed frequency of high output voltage (V_{FB}>2.05V typical). The efficiency and system cost are controlled at an optimal level. At light load, MX1210 enters the light load mode, where the output current is reduced. The switching losses are reduced by lowering the switching frequency.

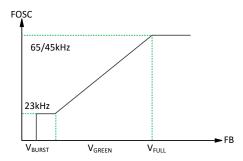


Fig2 FB voltage vs frequency

Current sensing and leading-edge blanking

Cycle by cycle current limiting is offered in MX1217E6 current mode PWM control. The switch current is detected by a sense resistor into CS pin. At internal leading-edge blanking circuit chops off the sensed voltage spike at initial internal power MOSFET on state due to snubber diode



reverse recovery and surge gate current of internal power MOSFET so that the external RC filtering on sense input is no longer needed. The current limiting comparator is disabled and cannot turn off the internal power MOSFET during the blanking period. The PWM duty cycle is determined by the current sense input voltage and the FB input voltage.

Internal synchronized slope compensation

Built-in slope compensation circuit adds voltage ramp into the current sense input voltage for PWM generation. This greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

Driver

The power MOSFET is driven by a dedicated gate driver for power switch control. Too weak the gate driver strength results in higher conduction and switch loss of MOSFET while too strong gate driver strength results the compromise of EMI.

A good tradeoff is achieved through the built-in totem pole gate design with right output strength and dead time control. The low idle loss and good EMI system design is easier to achieve with this dedicated control scheme.

Protection controls

Good power supply system reliability is achieved with auto recovery protection features including OCP, Under Voltage Lockout on VDD (UVLO) and over load protection, and latched shutdown features including VDD over voltage protection and output Over Voltage Protection (OVP).

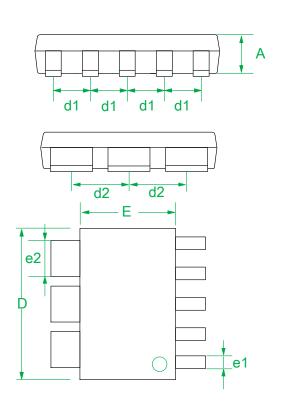
With MAXIN proprietary technology, the OCP is line voltage compensated to achieve constant output OCP limit over the universal input voltage range and its dependency on primary inductance and frequency is removed.

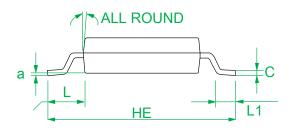
At overload condition when FB pin input voltage exceeds power limit threshold value for more than T_{D_OLP} , control circuit reacts to shut down the converter. It restarts when VDD voltage drops below UVLO limit.

When second rectifier diode shorted circuit, the voltage of current sense will be greater than 1.2V(typical), and then the internal MOSFET will be turn off, and the second rectifier diode short circuit protection can be achieved.

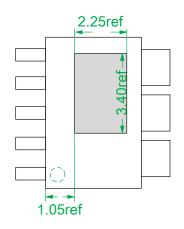


Package information





BOTTOM VIEW



CVMDOI		MILLIMETER	aS .	MIL		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	1.05	1.15	1.25	41	45	49
С	0.15	0.20	0.22	6	8	9
D	6.0	6.2	6.4	236	244	252
Е	3.7	3.9	4.1	146	154	161
HE	5.9	6.0	6.1	232	236	240
d1	1.25	1.30	1.35	49	51	53
d2	1.95	2.00	2.05	77	79	81
e1	0.35	0.40	0.45	14	16	18
e2	1.55	1.60	1.65	61	63	65
L	0.95	1.05	1.15	37	41	45
L1	040		0.80	16		31
a		0.2ref 8ref				
ALL ROUND		12°				

ESOP6 for MX1217E6



Restrictions on Product Use

- MAXIN micro is continually working to improve the quality and reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing MAXIN products, to comply with the standards of safety in making a safe design for the entire system, and to avoid situations in which a malfunction or failure of such MAXIN products could cause loss of human life, bodily injury or damage to property.
- ♦ In developing your designs, please ensure that MAXIN products are used within specified operating ranges as set forth in the most recent MAXIN products specifications.
- ◆ The information contained herein is subject to change without notice.

V10 The original version (preliminary) .